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COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 0-2 Sh. No. 0-1

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

DATE OF ORIGINAL ISSUE: NOV - 8 1966

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A Issue

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Cont. on Sh. 0-3 Sh. No. 0-2

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE OF CONTENTS

SECTION 1

	<u>Page</u>
1.0 General Description -----	1-1
1.1 Scope -----	1-1
1.2 GE-645 Prototype System Concept -----	1-1
1.3 Segmentation and Paging -----	1-3
1.4 GE-645 Prototype Processor Organization -----	1-3
1.5 Physical Description -----	1-6

SECTION 2

2.0 Functional Capabilities -----	2-1
2.1 Functional Description -----	2-1
2.2 Segmentation and Paging -----	2-2
2.2.1 Segmentation -----	2-2
2.2.2 Paging -----	2-5
2.2.3 Terms and Definitions -----	2-5
2.2.4 Access Rights -----	2-9
2.3 Modes of Operation -----	2-11
2.3.1 Definitions -----	2-11
2.3.2 Mode of Addressing(Absolute/Append) -----	2-11
2.3.3 Mode of Execution (Master/Slave) -----	2-12
2.4 GE-645 Prototype Processor Hardware Organization --	2-13
2.4.1 Physical Configuration -----	2-13
2.4.2 Modularity -----	2-13
2.4.3 Circuit Set -----	2-13
2.4.4 Interfaces -----	2-14
2.4.5 Processor Logic Organization -----	2-14

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE OF CONTENTS

SECTION 2 - contd

Page

2.4.5.1	Program Accessible Registers and Formats -----	2-17
2.4.5.2	Program Nonaccessible Registers and Formats-----	2-30
2.5	Information Representation-----	2-40
2.5.1	Number System -----	2-40
2.5.2	Processor Machine Word -----	2-41
2.5.3	Representation of Data -----	2-43
2.5.3.1	Alphanumeric -----	2-43
2.5.3.2	Numeric -----	2-44
2.5.4	Representation of Instruction, Indirect, and Indirect Then Tally Words -----	2-51
2.5.5	Appending Words -----	2-56
2.5.6	Associative Memory Word -----	2-58
2.6	Address Modification for Operands -----	2-63
2.6.1	Modification Types -----	2-63
2.6.1.1	Character Operations Specified by Address Modification -----	2-67
2.6.2	Address Modification Flowcharts -----	2-69
2.6.2.1	Flowchart Notation -----	2-69
2.7	Address Appending -----	2-84
2.7.1	General -----	2-84
2.7.2	Appending Cycle I -----	2-91
2.7.3	Appending Cycle II -----	2-92
2.7.4	Appending Cycle III -----	2-95
2.7.5	Appending Cycle IV -----	2-96
2.7.6	Appending Cycle V -----	2-99
2.7.7	Appending Cycle VI -----	2-99

COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
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PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh. 0-5 Sh. No. 0-4

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE OF CONTENTS

SECTION 2 contd

	<u>Page</u>
2.7.7.1 ITS -----	2-99
2.7.7.2 ITB -----	2-100
2.8 Instruction Repertoire -----	2-101
2.9 Faults and External Interrupts -----	2-101
2.9.1 Fault Categories -----	2-103
2.9.2 Fault Descriptions -----	2-104
2.9.3 Fault Priority -----	2-110
2.9.4 Fault Recognition -----	2-110
2.9.5 Fault Vector Address -----	2-111
2.9.6 Fault Sequence -----	2-112
2.9.7 Status Safestore and Restore -----	2-113
2.9.7.1 Correlation of Safestore Data with Safestore Status and Faults -----	2-115
2.9.8 Address and Pointer Generation for Groups V, VI -----	2-115
2.9.9 External Interrupts -----	2-115
2.9.9.1 External Faults -----	2-118
2.9.9.2 Interrupt Inhibit Bit -----	2-118
2.9.9.3 Lockup Fault -----	2-118
2.9.9.4 DIS -----	2-119
2.9.9.5 Interrupt Sampling Period -----	2-119
2.9.9.6 Address Generation For The Interrupt Vector -----	2-120
2.9.9.7 Processor Interrupt Mode -----	2-121
2.10 Instruction Execution Times -----	2-129
2.10.1 Basis For Calculation of The Listed Execution Times -----	2-129
2.10.1.1 Exceptions to Definition of "Average" -----	2-129
2.10.2 Address Modification and Appending Operation Times -----	2-131
2.10.3 Instruction Sequence Times -----	2-131
2.10.4 List of Instructions With Execution Times --	2-132

COMPANY CONFIDENTIAL
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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh. 0-6 Sh. No. 0-5

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE OF CONTENTS

<u>SECTION 3</u>	<u>Page</u>
3. 3.0 Operating Instructions -----	3-1
3.1 Maintenance Panel -----	3-1
3.1.1 Display Lights -----	3-1
3.1.1.1 Nonswitchable -----	3-3
3.1.1.2 Switchable -----	3-11
3.1.2 Switches -----	3-15
3.1.2.1 Switch Descriptions, Switch Panel -	3-15
3.1.2.2 Switch Descriptions, Main Panel ---	3-18
 <u>SECTION 4</u>	
4.0 Accuracy and Reliability -----	4-1
 <u>SECTION 5</u>	
5.0 Interface Requirements -----	5-1
 <u>SECTION 6</u>	
6.0 Installation Shipping and Storage Requirements ----	6-1

COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh. 0-7 Sh. No. 0-6

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

APPENDIX

		<u>Page</u>
Appendix A	Instruction Repertoire -----	A1
A-1	Description Format -----	A2
A-2	Abbreviations and Symbols -----	A4
A-3	Instruction Descriptions -----	A7
A-4	Index by Functional Class -----	A232
A-5	Alphabetical Index -----	A241

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

LIST OF FIGURES

SECTION 1

	<u>Page</u>
1.2 Simplified GE-645 Prototype System Block Diagram -----	1-2
1.4 GE-645 Prototype Processor, Configuration Block Diagram -----	1-5
1.5 GE-645 Prototype Processor Layout -----	1-7

SECTION 2

2.4.5 GE-645 Prototype Processor, Data Flow Block Diagram -----	2-15
2.5.2 The Machine Word -----	2-42
2.5.2a The Pair of Machine Words -----	2-42
2.5.3.1 Character Positions Within The Machine Word -----	2-43
2.5.3.2 Representation of Half-word, Single-word, and Double-word Precision, Numeric Formats -----	2-44
2.5.3.2a Representation of Floating-Point Numbers -----	2-47
2.5.4 Instruction and Indirect Word Format (except for IT modification) -----	2-51
2.5.4a Tag Field of Instruction and/or Indirect Word -----	2-52
2.5.4b Indirect Word for IT Modifications (except ITB or ITS) -----	2-53
2.5.4c Tag Format of Indirect Word for IT Modifications (except ITB and ITS --	2-54
2.5.4d ITB and ITS Word Formats in Memory-	2-55
2.5.5 SDW Word Format -----	2-56
2.5.5a PTW Format in Core Memory -----	2-57
2.5.6 Associative Memory Word Format -----	2-59
2.5.6a SDW in Associative Memory -----	2-60
2.5.6b PTW in Associative Memory -----	2-61

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

LIST OF FIGURES

SECTION 2 - contd

	<u>Page</u>
2.6.1.1 CI, SC, and SCR Modification Examples -----	2-68
2.6.2 GE-645 Address Modification Flow Chart -----	2-72
2.6.2a ITS/ITB Subroutine Flow Chart -----	2-74
2.6.2b SCR Subroutine, Flow Chart -----	2-75
2.6.2c AD Subroutine, Flow Chart -----	2-76
2.6.2d SO Subroutine, Flow Chart -----	2-77
2.6.2e ID Subroutine, Flow Chart -----	2-78
2.6.2f DI Subroutine, Flow Chart -----	2-79
2.6.2g Bit 29 Subroutine, Flow Chart -----	2-80
2.6.2h Fetch Subroutine, Flow Chart -----	2-81
2.6.2j SC Subroutine, Flow Chart -----	2-83
2.7.1 Address Spending Flow Chart -----	2-86
2.7.1a Parts of The Address Versus the 24-bit Core Address -----	2-90
2.9.9.6 Ingredients of XED Address Versus Fault and Interrupt Vector Tables in Memory -----	2-122
2.9.9.7 Interrupt Mode Flow Chart; Fault or Interrupt Recognition -----	2-123
2.9.9.7a Interrupt Mode Flow Chart; "Snapshot," Abort, Forced XED Sequence -----	2-124
2.9.9.7b Interrupt Mode Flow Chart; Execu- tion of First Instruction of Vector Pair -----	2-125
2.9.9.7c Interrupt Mode Flow Chart; Execu- tion of Second Instruction of Vector Pair -----	2-126

SECTION 3

3.1.1 GE-645 Maintenance Display Panel -----	3-2
3.1.2.1 Switch Panel -----	3-16
3.1.2.2 Top Part of Main Panel -----	3-19
3.1.2.2a Bottom Part of Main Panel -----	3-22

COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 0-10 Sh. No. 0-9

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

LIST OF TABLES

SECTION 2

Page

2.2.4	Segment Access Control Table -----	2-10
2.4.5.1	Program Accessible Registers and Formats -----	2-17
2.4.5.2	Program Nonaccessible Registers ---	2-30
2.5.3.2	Ranges of Fixed-Point Numbers -----	2-47
2.5.3.2a	Ranges of Floating-Point Numbers --	2-50
2.6.1	Types of Address Modification -----	2-64
2.6.1a	R, RI, and IR Register Designators-	2-65
2.6.1b	Tally Designators for IT Modification -----	2-66
2.9	GE-645 Faults -----	2-102
2.10.4	Instructions By Functional Class With Execution Times (50 foot cables) -----	2-133

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 0-11 Sh. No. 0-10

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE OF CONTENTS

<u>SECTION 7</u>		<u>PAGE</u>
	7.0 Physical Configuration-----	7-2
<u>SECTION 8</u>		
	8.0 Operational Description-----	8-1
<u>SECTION 9</u>		
	9.0 Control Unit Detailed Theory-----	9-1
	9.1 General Description-----	9-1
	9.1.1 Interface Lines Summary-----	9-2
	9.2 Modes and Sequences of Operation-----	9-14
	9.2.1 Sequence Control Flags-----	9-15
	9.2.1.1 Prepare (P) Flags-----	9-15
	9.2.1.2 Wait for Memory (W) Flags-----	9-16
	9.2.1.3 Even/Odd Sequence Flag--	9-17
	9.2.1.4 Auxiliary or Special Flags-----	9-18
	9.2.2 Instruction and Operand Address Modes-----	9-20
	9.2.2.1 Operand Address Modification	9-21
	9.2.3 Instruction Execution Modes-----	9-34
	9.2.3.1 MSI (Master in I- Register)-----	9-35
	9.2.4 Instruction Fetches-----	9-36
	9.2.5 Operand Fetches-----	9-39
	9.3 Principle Hardware Elements and Functions	9-43
	9.3.1 Strobe \$R, \$C, \$ΔAM1, \$ΔAM2, \$IF, and Interface Term-----	9-43

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 0-12 Sh. No. 0-11

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

SECTION 9TABLE OF CONTENTSPAGE

9.3.1.1	Strobe \$C and \$R Generation-----	9-44
9.3.1.2	Interface Term (INTR)---	9-48
9.3.1.3	Interface Term Inhibits-	9-52
9.3.1.4	Timing Diagram-----	9-56
9.3.2	Sequence Control Flags-----	9-58
9.3.2.1	Prepare Instruction (PI)	9-58
9.3.2.2	Prepare Address (PA)----	9-59
9.3.2.3	Prepare Address (PZ)----	9-61
9.3.2.4	Prepare Return or Repeat Indirect (PN)-----	9-62
9.3.2.5	Prepare IT Operand (PT)-	9-62
9.3.2.6	Prepare Rewrite (PR)----	9-62
9.3.2.7	Prepare Execute Interrupt (PC)-----	9-63
9.3.2.8	Wait for Operand (W)----	9-63
9.3.2.9	Wait for Instruction 1 (WI ₁)-----	9-64
9.3.2.10	Wait for Instruction 2 (WI ₂)-----	9-65
9.3.2.11	Wait for Indirect (WN)--	9-66
9.3.2.12	Even/Odd Sequence (ICF, ICG)-----	9-66
9.3.3	Interrupt Present Register (IPR)--	9-69
9.3.3.1	Interrupt Sampling-----	9-69
9.3.3.2	Reset Conditions-----	9-70
9.3.4	Input Data Control and Strobe Generation for the Y-, C- and I-Registers-----	9-70
9.3.4.1	Data-In-Control-----	9-72
9.3.4.2	Strobe \$YOC Generation--	9-77
9.3.4.3	Strobe Control for Y- and C-Registers-----	9-79
9.3.4.4	Strobe Generation for I-Register-----	9-81

COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 0-13 Sh. No. 0-12

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>SECTION 9</u>	<u>TABLE OF CONTENTS</u>	<u>PAGE</u>
9.3.5	ICT Strokes and Tracking Logic for ICTC, ICTB, ICTA' and ICTA Instruction Counters-----	9-81
9.3.5.1	Normal ICT Tracking-----	9-83
9.3.5.2	Fault Detected Tracking-----	9-85
9.3.5.3	RCU Instruction Tracking-----	9-86
9.3.6	CT-Register-----	9-86
9.3.7	RE-RO-Registers; \$ORY, \$ZOR and B Control-----	9-87
9.3.7.1	Status Flag-----	9-88
9.3.7.2	B Flip-Flop Control, \$ZOR Buffer and \$ORY Generation	9-91
9.3.7.3	Timing Diagram-----	9-93
9.3.8	MFREE Counter and MRD Control----	9-93
9.3.8.1	Count-Up Cycle-----	9-93
9.3.8.2	Count-Down Cycle-----	9-95
9.3.8.3	Timing Diagram-----	9-95
9.3.9	TMCH Counter-----	9-97
9.3.9.1	Count-Up Cycle-----	9-97
9.3.9.2	Count-Down Cycle-----	9-98
9.3.10	Store Compare (EX) Function-----	9-100
9.3.11	Z Function-----	9-103
9.3.12	Maintenance/Control Panel Functions	9-107
9.3.12.1	Switch Functions-----	9-107

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 0-14 Sh. No. 0-13

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

<u>SECTION 10</u>	<u>TABLE OF CONTENTS</u>	<u>PAGE</u>
10.0	Appending Unit Detailed Operation-----	10-1
10.1	Interface Frame Detailed Operation----	10-2
10.1.1	Function-----	10-3
10.1.2	Interface-----	10-9
	10.1.2.1 External-----	10-10
	10.1.2.2 Internal-----	10-16
10.1.3	Address Preparation-----	10-24
	10.1.3.1 Absolute Mode-----	10-24
	10.1.3.2 Append Without Associative Memory	10-26
	10.1.3.3 Append with Associa- tive Memory-----	10-37
10.1.4	Special Operation	10-42
	10.1.4.1 Written and Use Bits	10-42
	10.1.4.2 Descriptor Generator	10-61
	10.1.4.3 Base Instruction, Multiple Load Store	10-64
10.1.5	Memory Control-----	10-65
	10.1.5.1 Configuration and Interlace-----	10-65
	10.1.5.2 Port Selection Flip-Flops-----	10-72
	10.1.5.3 Command Logic-----	10-73
	10.1.5.4 Zone Lines-----	10-74
	10.1.5.5 Illegal Action Regis- ter (IAR)-----	10-75
	10.1.5.6 Data Out Register--	10-76
10.2	Base Frame Detailed Operation-----	10-79
10.2.1	General Description-----	10-79
	10.2.1.1 Interface Line Summary	10-80

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.0-15 Sh. No.0-14

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>SECTION 10</u>	<u>TABLE OF CONTENTS</u>	<u>PAGE</u>
	10.2.1.2 Register Formats-----	10-89
10.2.2	Basic Operating Cycles-----	10-91
	10.2.2.1 Base Frame Block Diagram--	10-91
	10.2.2.2 Appending Instructions (PI)	10-93
	10.2.2.3 Appending for Operands (PA,PZ,PN,PT)-----	10-93
	10.2.2.4 Wait for Modifier (WFM)--	10-96
	10.2.2.5 General Base Operations--	10-97
10.2.3	Operation Overlap-----	10-98
10.2.4	Strobe Generation-----	10-101
	10.2.4.1 External Strobe Utilization	10-101
	10.2.4.2 Internal Strobe Utilization	10-102
10.2.5	Increment Counter-----	10-103
10.2.6	Load Base Fault Detection-----	10-104
10.2.7	Even and Odd Segment Tag Registers (ESTR and OSTR)-----	10-104
10.2.8	Data In (ZDI) Switch-----	10-105
10.3	Detailed Operation-----	10-106
10.3.1	Appending Instructions (PI)-----	10-106
10.3.2	Appending Operands (PA,PZ,PN,PT)----	10-108
	10.3.2.1 Internal Base Selection--	10-108
	10.3.2.2 External Base Selection--	10-110
	10.3.2.3 ITS and ITB Reset-----	10-112
10.3.3	Wait for Modifiers (WFM) Operation--	10-113
10.3.4	General Base Operations-----	10-116
	10.3.4.1 Add to Base (ADB)-----	10-117
	10.3.4.2 Clear Associative ⁿ Memory (CAM)-----	10-119
	10.3.4.3 Store Associative Memory (SAM)-----	10-120
	10.3.4.4 Store Associative Memory Zero (SAZ)-----	10-122

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 0-16 Sh. No. 0-15

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>SECTION 10</u>	<u>TABLE OF CONTENTS</u>	<u>PAGE</u>
	10.3.4.5 Effective Address to Base _n (EABn)-----	10-124
	10.3.4.6 Effective Address to Pair _n (EAPn)-----	10-126
	10.3.4.7 Load Base Register n (LBRN)	10-129
	10.3.4.8 Load Base Registers (DLB)	10-131
	10.3.4.9 Load Descriptor Segment Base Register (LDBR)-----	10-131
	10.3.4.10 Load Control Field (LDCF)	10-134
10.4	Processor Power ON/Off Sequencing-----	10-136
10.5	Processor Fault Logic-----	10-136
	10.5.1 General Description-----	10-137
	10.5.1.1 Fault Descriptions-----	10-140
	10.5.1.2 Fault Detection and Recognition-----	10-140
	10.5.2 Fault Detection-----	10-149
	10.5.2.1 Group I Faults-----	10-149
	10.5.2.2 Group II Faults-----	10-149
	10.5.2.3 Group III Faults-----	10-150
	10.5.2.4 Group IV Faults-----	10-151
	10.5.2.5 Group V Faults-----	10-154
	10.5.2.6 Group VI Faults-----	10-156
	10.5.3 Fault Sequence Initiation-----	10-157
	10.5.3.1 SABL and SFF Level Generation-----	10-158
	10.5.3.2 Snapshot Counter-----	10-159
	10.5.3.3 Fault Address Encode-----	10-159

COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh. 0-17 Sh. No. 0-16

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>SECTION 11</u>	<u>TABLE OF CONTENTS</u>	<u>PAGE</u>
11.0	Associative Memory Unit Detailed Operation--	11-1
11.1	Function-----	11-2
11.1.1	SDW-----	11-2
11.1.2	PTW-----	11-4
11.1.3	Associative Memory Cycles-----	11-5
11.1.4	Associative Memory Instructions-----	11-7
11.1.5	Interface Signals-----	11-8
11.1.6	Manual Operation-----	11-10
11.2	Theory of Operation-----	11-11
11.2.1	Interface-----	11-11
11.2.2	Basic Operating-----	11-14
11.2.2.1	Search Cycle-----	11-14
11.2.2.2	Write Cycle-----	11-26
11.2.2.3	Read Cycle-----	11-27
11.2.2.4	Adjust Usage Counters Cycle-----	11-28
11.2.2.5	Clear Cycle-----	11-30
11.2.2.6	Termination-----	11-30
11.2.3	Associative Memory Instructions-----	11-31
11.2.3.1	SAZ(157)-----	11-31
11.2.3.2	SAM(557)-----	11-32
11.2.3.3	CAM(532)-----	11-34
11.2.4	Manual Operation-----	11-34
<u>SECTION 12</u>		
12.0	Operations Unit Detailed Operation-----	12-1
12.1	General-----	12-1
12.1.1	Functional Statement-----	12-1
12.2	OU Timing-----	12-3

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 0-18 Sh. No. 0-17

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>SECTION 12</u>	<u>TABLE OF CONTENTS</u>	<u>PAGE</u>
12.2.1	Basic "G" Cycles-----	12-8
12.2.1.1	GS-Setup or Start Cycle--	12-8
12.2.1.2	GO - General Operate Cycle	12-17
12.2.1.3	GC - Single Precision Store or First Half of a Double Precision Store Cycle-----	12-18
12.2.1.4	GT - Double Precision Store Operations Cycle---	12-18
12.2.1.5	GFT - Last Half of a Double Precision Store Cycle-----	12-18
12.2.1.6	GE - Floating Point Exponent Comparison Cycle	12-19
12.2.1.7	GA - Mantissa Alignment Cycle-----	12-19
12.2.1.8	GD1 - First Divide Opera- tions Cycle-----	12-19
12.2.1.9	GD2 - Second Divide Opera- tion Cycle-----	12-20
12.2.1.10	GN - Mantissa Normalization and/or Overshift Correction Cycle-----	12-21
12.2.1.11	GF - Final Cycle-----	12-21
12.2.2	Timing Pulse Generator-----	12-22
12.2.3	Timing Sequences-----	12-27
12.3	Instruction Description by Group-----	12-30
12.3.1	Fixed Point Add Group-----	12-30
12.3.1.1	Single Precision-----	12-33
12.3.1.2	Double Precision-----	12-62
12.3.2	Fixed Point Store Group-----	12-70
12.3.2.1	Single Precision-----	12-72
12.3.2.2	Double Precision-----	12-78
12.3.3	Read-Alter-Rewrite Group-----	12-82

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 00-19 Sh. No. 0-18

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>SECTION 12</u>	<u>TABLE OF CONTENTS</u>	<u>PAGE</u>
12.3.4	Shift Group-----	12-91
12.3.5	Fixed Point Multiply Group-----	12-104
12.3.6	Fixed Point Divide Group-----	12-118
12.3.7	Fixed Point Special Instruction Group	12-132
	12.3.7.1 RPT and RPL-----	12-133
	12.3.7.2 RPD-----	12-136
	12.3.7.3 BCD-----	12-138
	12.3.7.4 GTB-----	12-143
	12.3.7.5 LREG-----	12-147
	12.3.7.6 SREG-----	12-151
	12.3.7.7 CWL-----	12-155
	12.3.7.8 CMK-----	12-161
12.3.8	Floating Point Add Group-----	12-162
	12.3.8.1 Single Precision-----	12-164
	12.3.8.2 Double Precision-----	12-204
12.3.9	Floating Point Store Group-----	12-226
	12.3.9.1 Single Precision-----	12-226
	12.3.9.2 Double Precision-----	12-231
12.3.10	Floating Point Multiply Group-----	12-235
	12.3.10.1 Single Precision-----	12-235
	12.3.10.2 Double Precision-----	12-252
12.3.11	Floating Point Divide Group-----	12-254
	12.3.11.1 Single Precision-----	12-256
	12.3.11.2 Double Precision-----	12-269
12.3.12	Floating Point Special Instructions-	12-271
	12.3.12.1 FNO-----	12-271
	12.3.12.2 FNEG-----	12-276
12.4	G-Counter Description-----	12-278
12.4.1	G-Counter Control During Multiply, Divide and GTB Instructions-----	12-280

COMPANY CONFIDENTIAL.
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh. 0-20 Sh. No. 0-19

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>SECTION 12</u>	<u>TABLE OF CONTENTS</u>	<u>PAGE</u>
	12.4.1.1 Operation Cycles Required	12-280
	12.4.1.2 Fixed Count Insertion Control Equations-----	12-281
12.4.2	G-Counter Control During Shifts or Aligns-----	12-283
	12.4.2.1 Philosophy of Align Count Control During Floating Operations-----	12-283
	12.4.2.2 Equations for Transfer of Align Count from ES- to G-Counter-----	12-288
	12.4.2.3 Equations from Transferring the Number of Shift Counts to G-Counter-----	12-289
	12.4.2.4 G-Counter Decrement During Shifts or Align---	12-290
12.4.3	G-Counter Control During Normalize--	12-293
12.4.4	G-Counter Data Input Control-----	12-295
	12.4.4.1 General-----	12-295
	12.4.4.2 Conditional Complementary Set/Reset (CCSR) Control Requirements-----	12-297
12.5	Repeat Counter Description-----	12-298
12.6	Interval Timer Description-----	12-300
	12.6.1 General-----	12-300
	12.6.2 LDT-----	12-300
	12.6.3 Timer Runout-----	12-300
	12.6.4 STT -- SREG-----	12-301
12.7	The Indicators-----	12-302
	12.7.1 Zero Indicator-----	12-305
	12.7.2 Negative Indicator-----	12-305
	12.7.3 Carry Indicator-----	12-306

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 0-21 Sh. No. 0-20

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>SECTION 12</u>	<u>TABLE OF CONTENTS</u>	<u>PAGE</u>
	12.7.4 Overflow Indicator-----	12-306
	12.7.5 Exponent Overflow Indicator-----	12-306
	12.7.6 Exponent Underflow Indicator-----	12-307
	12.7.7 Overflow Mask Indicator-----	12-307
	12.7.8 Tally Runout Indicator-----	12-308
	12.7.9 Parity Error Indicator-----	12-308
	12.7.10 Parity Mask Indicator-----	12-309
	12.7.11 Absolute Mode Indicator-----	12-309
12.8	Special Control Flip-Flops-----	12-311
	12.8.1 Abort - Abort Cycle-----	12-311
	12.8.2 BCFF ₁ - BYTE Control-----	12-311
	12.8.3 BCFF ₂ -----	12-312
	12.8.4 BMFF - Byte Mode-----	12-313
	12.8.5 CMFF - Compare Magnitude-----	12-313
	12.8.6 DDF - Decode Delay Flag-----	12-314
	12.8.7 DIC - Data Inhibit Control-----	12-315
	12.8.8 DPFF - Double-Precision-----	12-315
	12.8.9 DUMF - Direct Modifier-----	12-316
	12.8.10 EIFF - Exponent Increment-----	12-317
	12.8.11 FRD - Repeat Double-----	12-318
	12.8.12 FTL - Repeat/Repeat Link-----	12-318
	12.8.13 GRU3, GRU2, GRU1-----	12-319
	12.8.14 H ₇₂ -----	12-320
	12.8.15 LAFF - Logical Align-----	12-320
	12.8.16 LAST-----	12-321
	12.8.17 N-1-----	12-321
	12.8.18 N36A-----	12-322
	12.8.19 N ₇₂ -----	12-322
	12.8.20 ORBF - Operation Register Busy-----	12-323
	12.8.21 ORYF - Operation Designator Ready-----	12-323
	12.8.22 OUBF - Operation Unit Busy-----	12-324
	12.8.23 Pass and PPS-----	12-324
	12.8.24 QSF - Quotient Sign-----	12-326
	12.8.25 REV - Reverse-----	12-327
	12.8.26 SDY ₁ and SDY ₂ - Store Ready-----	12-328
	12.8.27 Sense Term-----	12-329
	12.8.28 STFF - String-----	12-330
	12.8.29 YRY - Operand Ready-----	12-331

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 0-22 Sh. No. 0-213

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE OF CONTENTS

SECTION 12

PAGE

12.9	Last of 2, 3 OR n Pulse Detector-----	12-331
12.10	"S" Adder-----	12-333
12.10.1	General-----	12-333
12.10.2	Look Ahead Carry-----	12-337
12.10.3	Adder Modules-----	12-340
12.11	Flow Diagrams and Algorithm Description-----	12-349

SECTION 13

13.0	Maintenance-----	13-1
------	------------------	------

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 0-23 Sh. No. 0-22

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

LIST OF TABLES

SECTION 9

PAGE

9.1.1	Control Frame Inputs-----	9-3
9.1.1a	Control Frame Outputs-----	9-7
9.3.8.1	MFREE Counter States-----	9-95
9.3.9.1	TMCH Counter States-----	9-98
9.3.11	Comparison of Codes on ZT Bus with Codes in Z1, Z2 Registers-----	9-104

SECTION 10

10.1.2.1a	Zone Lines vs. Character and Bit Positions-----	10-11
10.1.2.1b	Memory Commands-----	10-13
10.1.2.2	Interface Frame Inputs-----	10-16
10.1.2.2a	Interface Frame Outputs-----	10-20
10.1.4.2	Resultant Descriptor for PTW-SDW Comparisons-----	10-63
10.1.5.1	Jumper Schedule for Various Memory Sizes-----	10-66
10.2.1.1	Base Frame Inputs-----	10-81
10.2.1.1a	Base Frame Outputs-----	10-84
10.5.1.1	Summary of Recognized Processor Faults-----	10-141
10.5.1.2	Groups I through VI Fault Detection and Recognition--	10-146

SECTION 11

11.2.1	Associative Memory Inputs-----	11-12
11.2.1a	Associative Memory Outputs-----	11-13
11.2.2.1	Search Possibilities vs. Pulses Generated and Sent to Interface Frame-----	11-15
11.2.2.2	Associative Register Bit Positions vs. Input Data Lines-----	11-27
11.2.3.2	Increment Counts vs. Register Stored for the SAM Instruction	11-33

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 0-24 Sh. No. 0-23

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>SECTION 12</u>	<u>LIST OF TABLES</u>	<u>PAGE</u>
	12.4.2.1 G-Counter Contents-----	12-286

COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 0-25 Sh. No. 0-24

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>SECTION 9</u>	<u>LIST OF FIGURES</u>	<u>PAGE</u>
	9.2.2.1 Address Modification in the GE-645 Flowchart-----	9-23
9.2.4	General Instruction Fetch Sequence Flowchart-----	9-37
9.2.5	Operand Fetches, Flowchart-----	9-41
	9.3.1.4 Major Control Unit Strokes Timing Diagram-----	9-57
9.3.5	Generalized ICT Tracking, Flowchart--	9-84
	9.3.7.3 RE, RO Buffer Loading, Timing Diagram-----	9-94
	9.3.8.3 MFREE Counter, Timing Diagram-----	9-96
 <u>SECTION 10</u>		
10.1.1	Absolute Mode Addressing, Flowchart--	10-4
10.1.1a	Append Without Associative Memory Flowchart-----	10-5
10.1.1b	Append With Associative Memory Flowchart-----	10-7
10.1.4	FAPM (AMS) Mode, Timing Diagram-----	10-49
10.1.4a	SWU (WBS) Mode, Timing Diagram-----	10-49
10.1.4b	SWU (WBS) Modes, Timing Diagram-----	10-50
10.1.4c	FAN (AMS) or PTW (AMS) Modes, Timing Diagram-----	10-50
10.1.4d	Descriptor Segment Page Table Word Fetch - Large Page, Flowchart-----	10-51
10.1.4e	Descriptor Segment Page Table Word Fetch - Small Page, Flowchart-----	10-52
10.1.4f	SDW Fetch Paged SWD Table (Large), Flowchart-----	10-53
10.1.4g	SDW Fetch, Paged SWD Table (Small), Flowchart-----	10-54
10.1.4h	SDW Fetch, Nonpaged Description Segment, Flowchart-----	10-55
10.1.4i	Page Table Word Fetch - Large Page, Flowchart-----	10-56

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 0-26 Sh. No. 0-25

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>SECTION 10</u>	<u>LIST OF FIGURES</u>	<u>PAGE</u>
10.1.4j	Page Table Word Fetch- Small Page, Flowchart-----	10-57
10.1.4k	Final Address Fetch Paged-Large Page, Flowchart-----	10-58
10.1.4m	Final Address Fetch Paged-Small Page, Flowchart-----	10-59
10.1.4n	Final Address Fetch Nonpaged, Flowchart-----	10-60
10.1.5.1	Jumper Card Layout-----	10-67
10.1.5.1b	Word Storage for Two 32K Memories with 02 Interlace-	10-69
10.1.5.1a	Port Selection for \$INT----	10-70
10.1.5.1c	Word Storage for Four 64K Memories with 0 Interlace--	10-71
10.1.5.2	Interrupt Address Formation	10-73
10.2.1.2	Base Frame, Register Formats	10-90
10.2.2.1	Base Frame Operations Flowchart for Appending PI: Appending PA, PZ, PN, PT and WFM Operation-----	10-92
10.2.3	Base Frame Operating Cycles in Relation to Control Frame Cycles-----	10-100
10.3.1	Appending Instructions (PI), Timing Diagram-----	10-107
10.3.2	Appending Operands (PA, PZ, PN, PT), Timing Diagram-----	10-109
10.3.3	Wait for Modifiers (WFM) Operations, Timing Diagrams-----	10-114
10.3.4.1	Add to Base n (ADBN), Timing Diagram-----	10-118
10.3.4.2	Clear Associative Memory (CAM) Timing Diagram-----	10-119
10.3.4.3	Store Associative Memory Instruction (SAM), Timing Diagram-----	10-121
10.3.4.4	Store Associative Memory Zero (SAZ) Timing Diagram--	10-123

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 0-27 Sh. No. 0-26

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>SECTION 10</u>	<u>LIST OF FIGURES</u>	<u>PAGE</u>
	10.3.4.5 Effective Address to Base n (EABn), Timing Diagram-----	10-125
	10.3.4.69 Effective Address to Pair n (EAPn), Timing Diagram-----	10-127
	10.3.4.7 Load Base Register n (LBRn) Timing Diagram-----	10-130
	10.3.4.8 Load Base Register (LDB) Timing Diagram-----	10-132
	10.3.4.9 Load Descriptor Segment Base Register (LDBR), Timing Diagram-----	10-133
	10.3.4.10 Load Control Field (LDCF) Timing Diagram-----	10-135
 <u>SECTION 11</u>		
	11.1.5 Associative Memory Interface Signals-	11-9
	11.2.2.1 No Match, Timing Diagram---	11-20
	11.2.2.1a Pointer Match for Large Page, No SDW or PTW Match, Timing Diagram-----	11-21
	11.2.2.1b SDW Match (nonpaged), Timing Diagram-----	11-22
	11.2.2.1c Match SDW for Small Page, Timing Diagram-----	11-23
	11.2.2.1d Match SDW for Large Page and PTW, Timing Diagram----	11-24
	11.2.2.1e Match PTW for Mall Page No SDW, Timing Diagram-----	11-25
 <u>SECTION 12</u>		
	12.2.1.1a Basic Control of the "GS" Cycle from Startup or OU Not Busy State-----	12-10
	12.2.1.1b Basic Control of the "GS" Cycle for Nonstore Instruc- tions with Instruction Overlap (Single Precision)-	12-14
	12.2.2 OU Pulse Generator-----	12-25

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 0-28 Sh. No. 0-279

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>SECTION 12</u>	<u>LIST OF FIGURES</u>	<u>PAGE</u>
12.2.3	OU Timing (G) Cycles-----	12-28
12.3.1	Major Data Paths and Control Points for the Fixed Point Add Type Instructions (OU)-----	12-31
12.3.1.1	LDA Instruction, Timing Diagram-----	12-35
12.3.1.1a	ADXn Instruction, Timing Diagram-----	12-39
12.3.1.1b	ORA Instruction, Timing Diagram-----	12-42
12.3.1.1c	Register Contents During GS Cycle of ORA Instruction---	12-43
12.3.1.1d	Register Contents During GF Cycle of ORA Instruction---	12-44
12.3.1.1e	CMG Instruction, Timing Diagram-----	12-47
12.3.1.1f	NEG Instruction, Timing Diagram-----	12-50
12.3.1.1g	ANA Instruction, Timing Diagram-----	12-54
12.3.1.1h	Register Contents During GS Cycle of ANA Instruction---	12-55
12.3.1.1i	Register Contents During GF Cycle of ANA Instruction---	12-56
12.3.1.1j	ADL Instruction, Timing Diagram-----	12-60
12.3.1.2	CANAQ Instruction, Timing Diagram-----	12-65
12.3.1.2a	SBAQ Instruction, Timing Diagram-----	12-69
12.3.2	Major Data Paths and Control Points for the Fixed Point Store Group of Instruc- tions (OU)-----	12-71
12.3.2.1	STQ Instruction, Timing Diagram-----	12-74
12.3.2.1a	STC1 Instruction, Timing Diagram-----	12-77
12.3.2.2	SMCM Instruction, Timing Diagram-----	12-81

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 0-29 Sh. No. 0-28

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>SECTION 12</u>	<u>LIST OF FIGURES</u>	<u>PAGE</u>
12.3.3	Major Data Paths and Control Points for the Read-Alter-Rewrite Group of Instructions (OU)-----	12-83
12.3.3a	AOS Instruction, Timing Diagram-----	12-87
12.3.3b	EROS Instruction, Timing Diagram-----	12-90
12.3.4	Major Data Paths and Control Points for the Shift Group of Instructions (OU)-	12-93
12.3.4a	ALS Instruction, Timing Diagram-----	12-99
12.3.4b	LLR Instruction, Timing Diagram-----	12-103
12.3.5	Major Data Paths and Control Points for the Fixed Point Multiply Instructions (OU)-----	12-105
12.3.5a	MPF Instruction, Timing Diagram-----	12-116
12.3.6	Major Data Paths and Control Points for the Fixed Point Divide Instruction	12-119
12.3.6a	DIV Instruction, Timing Diagram-----	12-130
12.3.7.1	RPT/RPL Instructions, Timing Diagram-----	12-135
12.3.7.2	RPD Instruction, Timing Diagram-----	12-137
12.3.7.4	GTB Instruction, Example---	12-146
12.3.8	Floating Point Add Group, Major Flowchart-----	12-163
12.3.8.1	FAD Instruction, Timing Diagram-----	12-172
12.3.8.1a	Register Contents During GS, GF Cycles of FAD Instructions	12-173
12.3.8.1b	Register Contents During GA, GO Cycles of FAD Instructions-----	12-174
12.3.8.1c	Register Contents During GN Cycle of FAD Instruction---	12-175
12.3.8.1d	Register Contents During GF Cycle of FAD Instruction---	12-176
12.3.8.1e	FLD Instruction, Timing Diagram-----	12-180

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 00-30 Sh. No. 0-0-29

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>SECTION 12</u>	<u>LIST OF FIGURES</u>	<u>PAGE</u>
12.3.8.1f	ADE Instruction, Timing Diagram-----	12-183
12.3.8.1g	FCMG Instruction, Timing Diagram-----	12-190
12.3.8.1h	Register Contents During GS, GE Cycles of FCMG Instruc- tion-----	12-191
12.3.8.1i	Register Contents During GA, GE Cycles of FCMG Instruction-----	12-192
12.3.8.1j	UFS Instruction, Timing Diagram-----	12-200
12.3.8.1k	Register Contents During GS GE Cycles of UFS Instruction	12-201
12.3.8.1m	Register Contents During GA, GO Cycles of UFS Instruction-----	12-202
12.3.8.1n	Register Contents During GF Cycle of UFS Instruction	12-203
12.3.8.2	DFSB Instruction, Timing Diagram-----	12-213
12.3.8.2a	Register Contents During GS, GE Cycles of DFSB Instruction-----	12-214
12.3.8.2b	Register Contents During GO, GN Cycles of DFSB Instruction-----	12-215
12.3.8.2c	Register Contents During GF Cycle of DFSB Instruction	12-216
12.3.8.2d	DFCMP Instruction, Timing Diagram-----	12-222
12.3.8.2e	Register Contents During GS, GE Cycles of DFCMP Instruction-----	12-223
12.3.8.2f	Register Contents During GA Cycle of DFCMP Instruction-	12-224
12.3.8.2g	Register Contents During GF Cycle of DFCMP Instruction-	12-225

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 0-313 Sh. No. 0-30

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>SECTION 12</u>	<u>LIST OF FIGURES</u>	<u>PAGE</u>
12.3.9	Floating Point Store Group, Major Flowchart-----	12-227
12.3.9.1	FST Instruction, Timing Diagram-----	12-230
12.3.9.2	DFST Instruction, Timing Diagram-----	12-234
12.3.10	Floating Point Divide Group, Major Flowchart-----	12-236
12.3.10.1	FMP Instruction, Timing Diagram-----	12-250
12.3.11	Floating Divide Group Registers and Data Flow-----	12-225
12.4.4.1	Conditional Complementary Control Block Diagram-----	12-296
12.9	Last of 2, 3 or n Pulse Detector, Logic Diagram---	12-332
12.10.1	S Adder Function Block-----	12-335
12.10.2	Byte Carry Detector LOM306A-----	12-339
12.10.3a	LM303A Adder, Block Diagram-----	12-340
12.10.3b	LM303A Ki+1 Control, Logic Diagram---	12-342
12.10.3c	LM303A Ci+1 Carry, Logic Diagram-----	12-342
12.10.3d	LM303A Ci Carry, Logic Diagram-----	12-343
12.10.3e	LM303A Sum _i +1, Logic Diagram-----	12-344
12.10.3f	LM304A, Block Diagram-----	12-346
12.10.3g	LM304A Ci+1 Carry, Logic Diagram-----	12-346
12.10.3h	LM304A Ci Carry, Logic Diagram-----	12-347
12.11	Flow Diagram for MPY (Integer Multiply)-----	12-350
12.11a	Flow Diagram for DIV (Integer Divide)-----	12-351
12.11b	Flow Diagram for BCD (Binary to Binary Coded Decimal)-----	12-353
12.11c	Flow Diagram for FAD (Floating Add)-----	12-354

COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 1-1 Sh. No. 0-31

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

INTRODUCTION

This Engineering Product Specification (EPS) defines and describes the requirements and design implementation of a multiple-access time-shared computer designated the GE-645 Prototype; specifically the GE-645 Prototype Processor. Information and interfaces relating to the total GE-645 Prototype System are included within this EPS only in the detail necessary to define or explain the Processor design requirements.

The information contained within this EPS is divided into two major parts: Part I - Performance Specification and Part II - Design Specification. Part I contains the general over-all design requirements and parameters that define the GE-645 Prototype Processor: general description, functional specifications, operation, accuracy and reliability, interface requirements, installation shipping, and storage requirements. Part II documents the design implementation of the requirements outlined in Part I and includes: physical configuration, general Processor theory of operation, detailed Processor theory of operation, maintenance design, and test requirements.

It will be noted that many areas of this specification reference the Engineering System Specification (ESS) M50EB00105 for the GE-645 Prototype System. This EPS is not considered complete without the information contained in the ESS. Where any apparent conflicts exist between these two specifications, the EPS shall apply.

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Spec. No. M50EB00107

Cont. on Sh. 1-2 Sh. No. 1-1

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

PART I - PERFORMANCE SPECIFICATION

1.0 GENERAL DESCRIPTION

1.1 SCOPE

This section contains information to present a general picture of the GE-645 Prototype Processor and its relationship to the total GE-645 Prototype System. The system configuration and objectives are discussed only in enough detail to place the Processor in proper perspective, and explain some of the reasons for the Processor hardware organization.

1.2 GE-645 PROTOTYPE SYSTEM CONCEPT

The basic idea behind the GE-645 Prototype System, is that it is a system somewhat analogous to a public utility; that is, the System allows direct access problem-solving (data processing, etc.) to a large computer from any type of remote terminal device, at any time, for a large number of users on a time-sharing basis. To provide this kind of service on an efficient economic basis to multiple users requires a system that is memory orientated with a hierarchy of memory devices that allows the user "...multiple access to a vast common structure of data and program procedures," on an "as needed" basis. The hardware organization of the total GE-645 Prototype System reflects the need for vast amounts of memory of varying speed and capacity. It should be noted as shown on Fig. 1.2 that except for additional memory capacity, the System is configured almost exactly like the GE-625/635 System. The difference lies primarily within the Processor, which has been expanded considerably to augment the basic 625/635 Processor in the area of memory addressing (24 bits for 16 M words), memory management, segmentation, and "page turning" for core, drum, disc, and tape combinations.

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Spec. No. M50EB00107

Cont. on Sh.1-3 Sh. No.1-2

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

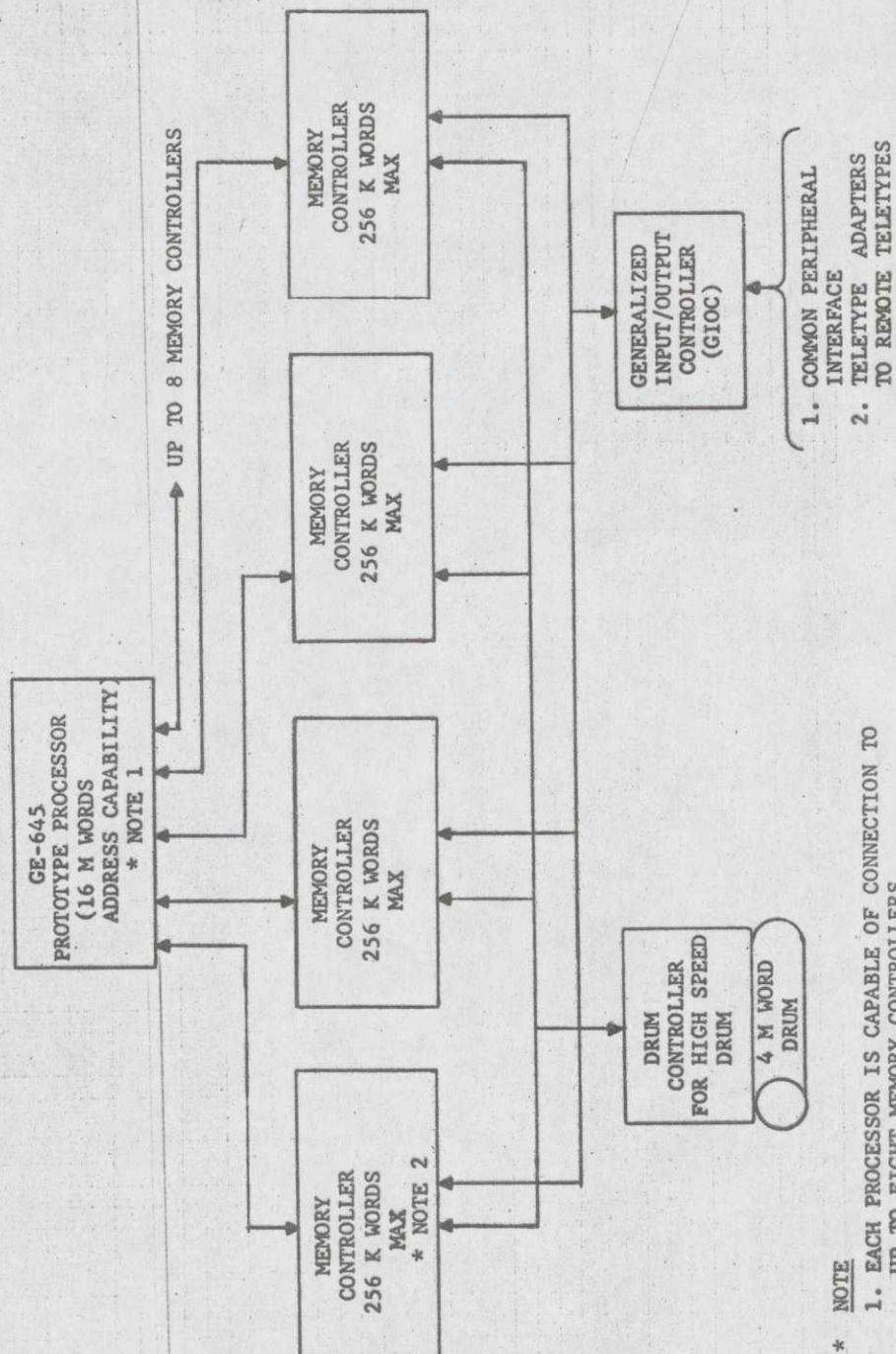


FIG. 1.2 SIMPLIFIED GE-645 PROTOTYPE SYSTEM BLOCK DIAGRAM

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

1.2 - contd

Hardware within the GE-645 Prototype Processor provides the capability and flexibility for the design of an efficient software system. Such a software system is required for dynamic memory relocation and scheduling of many "users" on an economical real-time, time-shared basis.

The total GE-645 Prototype System configuration is extremely flexible both in a multiprocessing or multiprogramming environment, depending on specific requirements of the intended user. This information, if desired in detail, may best be obtained from the GE-645 Engineering System Specification (ESS) M50EB00105.

1.3 SEGMENTATION AND PAGING

The GE-645 employs a method of addressing called appending, (for instructions and operands) to fulfill system requirements for Segmentation and Paging of the memory hierarchy. The detailed requirements placed on the Processor Module are covered in paragraph 3.5.8 of the ESS and paragraphs 2.2 and 2.7 of this specification.

1.4 GE-645 PROTOTYPE PROCESSOR ORGANIZATION

To implement the dynamic relocation and memory segmentation concept in the GE-645; the Processor shall be organized in four relatively modular units as shown on Fig. 1.4; the Control Unit, Operations Unit, Appending Unit, and the Associative Memory Unit. The major functions which shall be performed by each of the four modular units are summarized as follows:

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Spec. No. M50EB00107

Cont. on Sh. 1-5 Sh. No. 1-4

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

1.4 - contd

Control Unit

- All Processor control functions
- Address modification
- Mode of operation (Master/Slave and Absolute/Append)
- Interrupt recognition
- Operation decoding

Operations Unit

- Fractional and integer divisions and multiplications
- Automatic alignment of floating-point numbers for additions and subtractions
- Inverted divisions on floating-point numbers
- Automatic normalization of floating-point resultants
- Separate operations on the exponents and mantissas of floating-point numbers
- Shifts
- Indicator Register loading and storing
- Timer Register loading and decrementing
- Normal arithmetic operations
- All logical operations

Appending Unit

- Data input/output to memory
- Memory configuration and interlace
- Address appending
- Fault recognition
- Power on/off sequencing

Associative Memory Unit

- Contains Segment Descriptor and/or Page Table Words on a most actively used basis. Eliminates the need for possible multiple memory accesses before obtaining an absolute memory address of a word. Capability of referencing 4 M of core memory.

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Spec. No. M50EB00107

Cont. on Sh. 1-6 Sh. No. 1-5

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

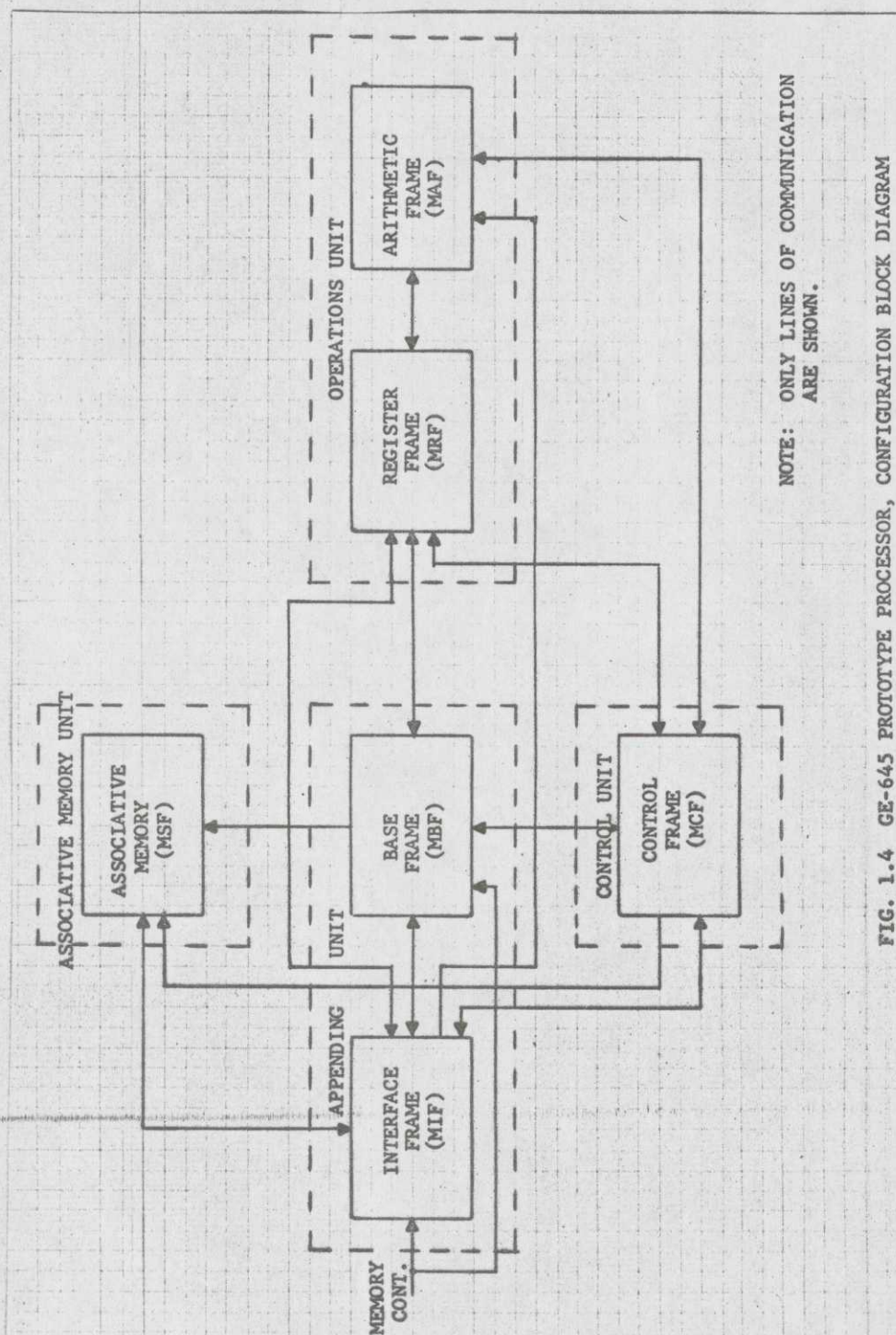


FIG. 1.4 GE-645 PROTOTYPE PROCESSOR, CONFIGURATION BLOCK DIAGRAM

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

1.4 - contd

Details of the GE-645 Prototype Processor data flow are illustrated on Fig. 2.4.4 in Section 2 and the various functional parts that comprise each of the four units are explained.

1.5 PHYSICAL DESCRIPTION

The GE-645 Prototype Processor shall consist of six frames of component boards contained within a cabinet that is standard Computer Equipment Department height and width, but approximately twice as long. All external signal and power cables shall come into the Processor Cabinet via an eight-port "snowplow." Power supplies for the six frames shall be located in the middle of the cabinet and behind the Maintenance Panel; the Maintenance Panel is located at the opposite end of the cabinet from the "snowplow." A relay module for the display lights on the Maintenance Panel is located on the opposite end of the cabinet from the Maintenance Panel. Cooling is accomplished via eight blowers located in the bottom of the cabinet and one blower located between power supplies in back of the Maintenance Panel; the cooling air exhausted at the top. The physical configuration of the six frames within the Processor Cabinet, and the arrangement of modules and "buckets" within each frame is shown on Fig. 1.5 and shall conform to Computer Equipment Department Standards on Physical Device Location and Pin Nomenclature. Physical details of the Processor are included in Part II of this EPS and Section 6.0 of the ESS.

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

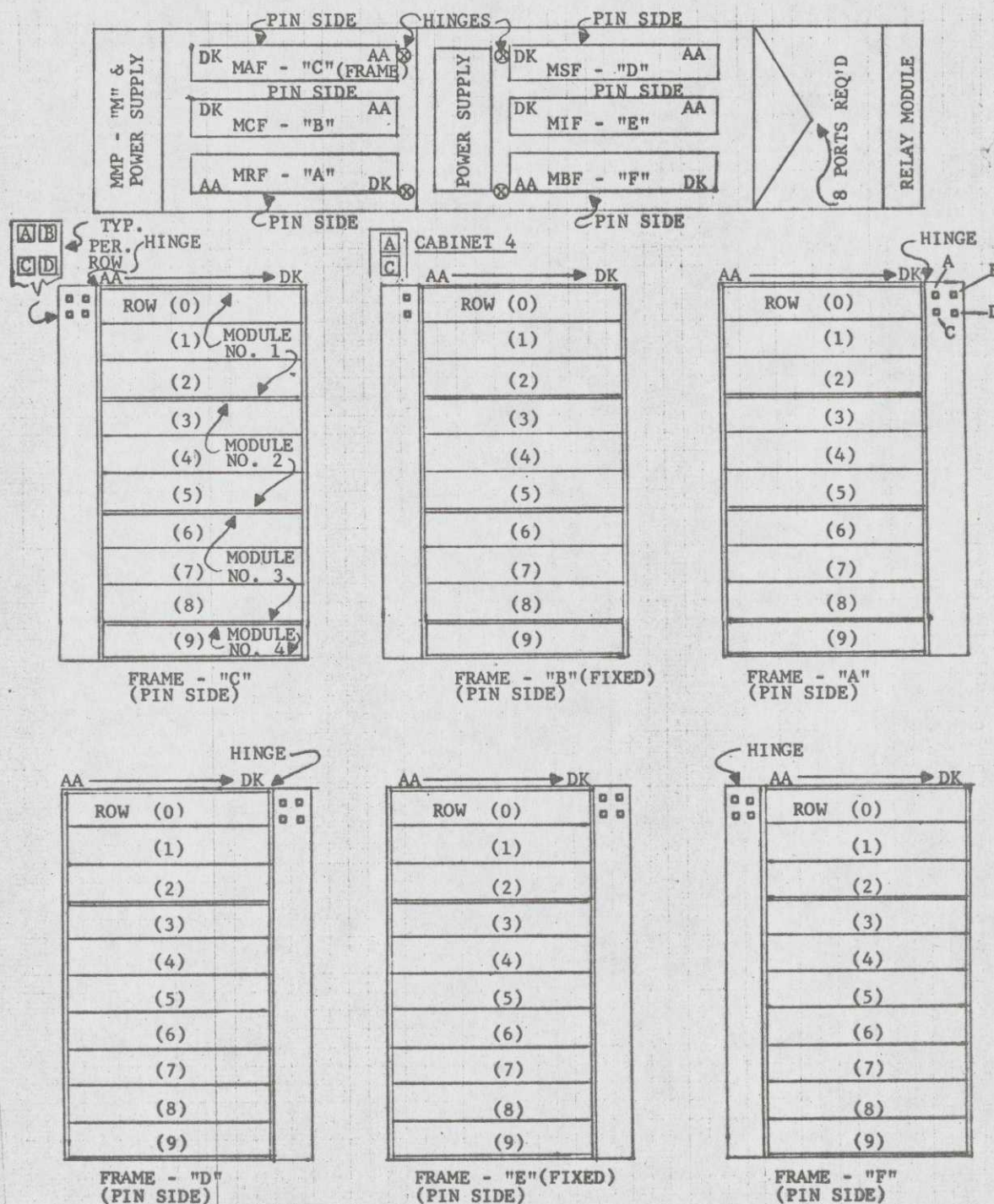


FIG. 1.5 GE-645 PROTOTYPE PROCESSOR LAYOUT

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Spec. No. M50EB00107

Cont. on Sh. 2-2 Sh. No. 2-1

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.0 FUNCTIONAL CAPABILITIES

This section is a further definition of the functional requirements for the GE-645 Prototype Processor that are spelled out in general terms in the 645 Engineering System Specification (ESS) M50EB00105. Information contained in the ESS is either referenced or mentioned briefly; the main emphasis is on the hardware requirements that must be specified in detail for the GE-645 Prototype Processor.

2.1 FUNCTIONAL DESCRIPTION

The functional description of the GE-645 Prototype Processor Module is covered in general terms in paragraph 3.5 of the 645 ESS. A brief listing of the information in the ESS is presented below with the applicable paragraph numbers in parenthesis:

- General (3.5.1)
- Physical Configuration (3.5.2)
- Modularity (3.5.3)
- Circuit Set (3.5.4)
- Interfaces (3.5.5)
- Program Accessible Register (3.5.6)
- Information Representation (3.5.7)
- Segmentation and Paging (3.5.8)
- Operating Modes (3.5.9)
- Address Modification (3.5.10)
- Instruction Repertoire (3.5.11)
- Instruction Execution Times (3.5.12)
- Faults and Interrupts (3.5.13)
- Manual Control and Indicators (3.5.14)
- Maintenance (3.5.15)

Other paragraphs in the ESS contain information that pertains to the functional description of the Processor Module. These applicable areas shall be extracted or referenced as necessary when first mentioned.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.2 SEGMENTATION AND PAGING

The concepts and specifications for segmentation and paging in the GE-645 are outlined in detail in paragraph 3.5.8 of the 645 ESS. The general philosophy will be repeated here as an introduction to the hardware implementation of the aforementioned concepts, and presented in paragraph 2.7 - Address Appending.

2.2.1 SEGMENTATION

Segmentation refers to the concept of dividing a program into self-contained parts in order to be able to execute the program without maintaining it in its entirety in memory at any one time.

A segment is a collection of instructions and/or data which are all associated with a particular segment name.

A subroutine, such as a square root subroutine, can be written as a segment. Now many users can incorporate the subroutine in their process by specifying the segment name. The user does not need to describe or copy the individual instructions. Similarly, data may be shared among many users by each user specifying the name of the data segment.

Occasionally, a procedure segment will be found to have an error in it. Or, a need will arise for having the segment do more or do things in a better way. The segment is changed and recompiled or reassembled. Usually, the new version will perform the same functions as the old version and with the same interface to the user. When this is the case, the program which used the old segment needs no changes in order to use the new segment.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.2.1 - contd

Since segments are relatively independent of each other, many people can be preparing segments at the same time. Symbolic names can be used freely. Obviously, when an instruction in segment A refers to a word in segment B, the segment A instruction must know the name of segment B and the name of the desired word in segment B. The important point is that the choice of names for the words in segment B does not need to be coordinated with the writers of other segments, except for those names referred to by other segments.

Communication between segments is done via symbolic names. Therefore, a segment does not have to be in specific memory locations.

There is no requirement for all the segments which belong to a program to be in memory at the same time. Hence, segments which are not being used do not occupy valuable main memory space.

Another way to save memory is to use pure procedure segments. These are segments which do not modify themselves. They are written in a re-entrant, recursive manner. Therefore, all programs can use the same copy of a pure procedure segment. Thus, only one copy of the segment is needed in memory, rather than one copy for every program which uses that segment. A further definition of this concept is contained in section 2.1.4 of the ESS.

The major reasons for segmentation are as follows:

- 1) The user with segments is able to program in an essentially infinite memory system. Any one segment can contain up to a quarter million words. On the GE-645, any single segment can dynamically grow or shrink between the limits of 64 to 256 K words.
- 2) The user can operate his program through phases of segment configuration without prior planning of the storage allocation needs of the management of the segments.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.2.1 - contd

- 3) The largest amount of code which must be bound together as a solid block is a single segment. Since binding pieces of code together is a process which is similar to assembly or compiling, the advantage is immense of being able to prepare arbitrarily large programs out of a series of segments connected by an efficient binding method.

The segmentation description points out that a segment does not always have to be in the same memory locations. Nor do all segments for a program have to be in memory at the same time. The paging concept carries these ideas even further, in that not all of the pages which comprise a segment need be in memory at the same time. This idea is elaborated on below.

Assume for a moment that all the pages of some segment are stored in memory. Now think of the memory occupied by this segment as being partitioned into several blocks, all the same size. The segment can be paged into several pages, each of which contains the same number of words as the memory block size. (The actual block sizes available in the system are 64 words and 1024 words.)

The essential point of the paging concept is that the pages of a given segment need not be located in contiguous memory blocks.

As pages are needed, they are retrieved from secondary storage. The pages are placed in any available block of main memory. The linking of the new pages to the ones already in memory is discussed in Section, 2.1.3. of the ESS.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.2.1 - contd

Eventually, the memory will be full and more pages will be needed. Some pages are going to have to be displaced. However, if a page which is no longer needed is part of a pure procedure segment, or if the page has never been written into, the operating system does not have to write out the page. The page is still in the secondary storage. Any access controls which were established for a segment obviously apply to the pages which make up that segment. However, an individual page within a segment may have more restrictive access controls.

2.2.2 PAGING

Paging has two distinct advantages:

- 1) It allows a flexible technique of dynamic storage management and reduces overhead which is especially high in heavy-traffic situations such as occur in responsive time-sharing systems.
- 2) The mechanism of paging as implemented in the GE-645 allows the operation by only a portion of the pages of a segment so that by only retaining active pages more effective use can be made of high-speed memory.

The combined abilities of an Operating Supervisor and the hardware features of the GE-645 will allow all of this relocation, paging, linkage, and protection to take place.

2.2.3 TERMS AND DEFINITIONS

The following terms and definitions peculiar to segmentation are listed to assist the reader in understanding subsequent discussions and descriptions presented in later paragraphs and sections of this EPS.

Absolute Address Base -- the core memory address of the first location of the page or segment being referenced.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.2.3 - contd

Appending

- uniting and/or linking specific combinations of Base Registers, Segment Descriptor Words, Page Table Words and effective addresses to form an absolute memory address. Also, the uniting of relative addresses to base addresses to develop effective addresses and pointers. The term appending also infers a simultaneous verification that the address is within limits and that other access criteria are met.

Associative Memory

- high-speed memory used in appending which contains recently referenced segment and page locations and other related information. (See 2.5.6 for word formats.)

Base Registers
(ABR, PBR, TBR
See Paragraph 2.4.5
for details)

- used to augment an instruction, indirect, or operand word address in all cases, except possibly the Absolute mode. Also used as a pointer to the descriptor segment.

Descriptor Segment

- a list of words which is used as an index to point to segments or to segment page tables, and describes the size of such segments and the restrictions on their access.

Effective Address

- refers to the combined page number and word number, formed from the instruction word, any address modification and an internal base if appending was specified, thus providing logically sequential addresses to the user while the absolute address used to access memory may be quite different.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.2.3 - contd

- | | |
|-----------------------|--|
| External Base | - an Address Base Register used to reference a segment outside of the procedure segment being executed. It will be referenced either from an internal base control field or the segment tag. |
| Internal Base | - an Address Base Register used to reference a location within a segment. It contains an address which is relative to the external base specified by this base register. |
| K | - One thousand twenty-four (1024). |
| Page | - a fixed subdivision of addresses within a segment. The page size must be either 64 or 1024 words, and a page always starts at an address which is an integer multiple of the page size. The maximum number of pages within a segment is 256. |
| Page Table | - a set of words associated with a segment which contains the absolute base address of the pages and an access control field. |
| Page Table Word (PTW) | - a word contained in the page table which points to the absolute address base (modulo 64/1024) of the page in memory and an access control field. (See 2.5.5 for word formats.) |

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.2.3 - contd

Pointer

- a linkage value used as an intermediate address or address modifier to locate an address to access the particular word(s) to be used. An Address Base Register, an indirect word, or an Index Register are specific examples of what can be used as a pointer or part of a pointer.

Procedure Segment

- a segment which consists primarily of instructions. A procedure segment is considered "pure" if it is unaltered by execution.

Process

- a sequence of execution of procedures including the data referenced by the procedures. The sequence may or may not be altered during execution.

Relative Addressing

- relative memory addresses are assigned sequentially from location zero during program assembly or compilation. It is intended that these addresses be relocated by a convenient value or values at load time and/or execution time.

Segment

- an ordered set of words referenced by a unique name. The segment may consist of instructions and/or data words. It has a fixed length but the portion of it contained in memory during execution may vary. The maximum addressable segment length is 256k.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 2-10 Sh. No. 2-9

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.2.3 - contd

- Segment Descriptor Word (SDW) - a word which contains the absolute address base (modulo 64/1024) of a segment in memory, a size field, and an access control field. (See 2.5.5 for word formats.)
- Segment Tag - this tag, when used, consists of the three most-significant bits of the instruction word. It specifies one of eight Address Base Registers to be used in appending.
- Segment Tag Registers - two registers which contain the segment tags (and bit 29 of the instruction word when it is a one) of the even and odd instruction words.

2.2.4 ACCESS RIGHTS

Since the GE-645 Prototype System has the capability for servicing many users at the same time, the question of access rights to certain areas of segments and pages within segments is quite important. All question of access rights to segments and pages within segments is controlled by the Operating System (Multics-645/I). The Operating System shall perform this function by setting certain control bits in the SDW and PTW linkage words. A definition of the control information in the SDW and PTW words is presented in paragraph 2.5.5. What this means in terms of access to segments or pages is shown in Table 2.2.4.

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Spec. No. M50EB00107

Cont. on Sh. 2-11 Sh. No. 2-10

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Table 2.2.4 Segment Access Control Table

Current Procedure Mode	Control Bits in SDW or PTW of Segment Being Accessed			Access Permitted			
				Non-Transfers		Same Segment	Different Segment
	Class (Bits 33-35)	Access (Bit 31)	Write (Bit 30)	Read	Write	TBR=PBR	TBR≠PBR
Master	Data Segment (001)	0/1	0/1	Yes	Yes	No	No
	Procedure Slave(010)	0/1	0/1	Yes	Yes	Yes	Yes
	Execute(011) Master(100)						
Slave	Data Segment (001)	0	0/1	No	No	No	No
		1	0	Yes	No	No	No
		1	1	Yes	Yes	No	No
	Procedure Slave(010)	0	0/1	No	No	No	No
		1	0	Yes	No	Yes	Yes
		1	1	Yes	Yes	Yes	Yes
	Procedure Execute Only (011)	0	0/1	No	No	No	No
		1	0	①	No	Yes	②
		1	1	①	①	Yes	②
	Procedure Master (100)	0	0/1	No	No	No	No
		1	0/1	No	No	No	②

NOTE: ① If PBR=TBR then yes; else no.

② If Effective Address=0 then yes; else no.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.3 MODES OF OPERATION

2.3.1 DEFINITIONS

The modes of operation within the GE-645 Prototype Processor refer to the modes of execution (which has to do with the privileges of executing certain instructions and with access rights), and the mode of addressing (which has to do with generation of a core location corresponding to an effective address specified by the program). In the GE-645, addressing and execution modes are handled separately; the addressing mode specified by the Absolute flip-flop which is included as bit 28 of the Indicator Register; the execution mode specified by the Master/Slave flip-flop which is set according to the Descriptor of the current procedure. The Master/Slave flip-flop is not included in the Indicator Register, as it was in the GE-625/635.

2.3.2 MODE OF ADDRESSING (Absolute/Append)

In the Absolute mode the effective address becomes the core location (that is, absolute address). This is always the case for instruction fetch, $ICTB_{0-17} \Rightarrow ADR_{6-23}, 00...00 \Rightarrow ADR_{0-5}$. The appending mechanism is bypassed. Addresses are limited to the bottom 256k of memory. Absolute mode may be viewed as the creation of a segment whose base address is all zeros, which replaces the segment defined by the PBR. The intersegment fetch of indirect words and operands is optional through the use of bit 29 of the instruction word, or ITB, ITS modifiers. In other words, indirect words and operands may be addressed in absolute or via appending.

In the Append mode, the appending mechanism is employed for all instruction, indirect words, operand fetches. The effective address is either added to a base address (nonpaged), or its word number field is concatenated to the base address (paged).

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.3.2 - contd

The Control Unit is normally in the Append mode but the Absolute mode is entered temporarily when an XED instruction pointing to a fault or interrupt vector is "brute forced." The mode will become Absolute if either instruction is a satisfied transfer, other than TSS, without bit 29 = 1 or ITB, ITS indirection. The Control Unit remains in Absolute until TSS is executed or a transfer with bit 29 = "1" takes place.

The Absolute mode may also be entered or exited if in Master mode one of the following instructions brings a different state in the bit position corresponding to the Absolute indicator (bit 28 of the IR): RET, RTD, RCU.

2.3.3 MODE OF EXECUTION (Master/Slave)

In the Master mode, any instruction in the GE-645 repertoire may be executed. All classes of information may be accessed regardless of the Access bit and the Write Permit bit. The only access restriction is that the data class may not be accessed for instruction fetches. Bit 28 (interrupt inhibit) is effective in Master mode. The Timer Runout fault is ignored in Master mode.

In the Slave mode, an attempt to execute privileged instructions, or semiprivileged instructions contrary to lock bit convention results in an Illegal Procedure fault. All accesses are controlled by the Access and Write Permit bits and the class of the current procedure and target segments (for details see the Appending Cycle Flow Chart in 2.7).

If the Descriptor (bits 27-35 of the Segment Descriptor Word) of the current procedure is Procedure-Master, then the mode is Master, if the descriptor is Procedure-Slave, or Procedure-Execute only, then the mode is Slave. In general, the mode is in effect until the next instruction fetch. In the Absolute addressing mode (or temporary Absolute) there are no procedure descriptors and the execution mode is defined as Master.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.3.3 - contd

The Master mode may be exited by an RCU instruction which brings a zero in the bit position corresponding to the Master/Slave status flag (bit 33 in $C(Y + 3)$) of the Control Frame status words stored by an SCU instruction.

2.4 GE-645 PROTOTYPE PROCESSOR HARDWARE ORGANIZATION

The Engineering System Specification and Section 1.0 of this specification specify the four major functional units that make up the Processor Module. The following paragraphs deal specifically with the hardware organization within each of the major functional units.

2.4.1 PHYSICAL CONFIGURATION

The physical arrangement of the four functional units into frames of logic, and the designation of these frames is covered in paragraph 1.5 and GE-drawing 43E160145.

2.4.2 MODULARITY

The GE-645 Prototype Processor shall be designed as a modular item conforming to the definition of an "Active Module" as defined by the GE-645 ESS. The definitions of memory interface, and the memory port selection logic for eight memory ports shall apply.

2.4.3 CIRCUIT SET

The Processor shall use only the standard 600-line circuit set whose specifications are contained in the Computer Equipment Department "Electronic Standards Handbook, Volume IV." New circuits developed specifically for particular GE-645 Prototype Processor applications shall conform to 600-line standards and shall be included in the aforementioned handbook.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.2-15 Sh. No.2-14

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.4.4 INTERFACES

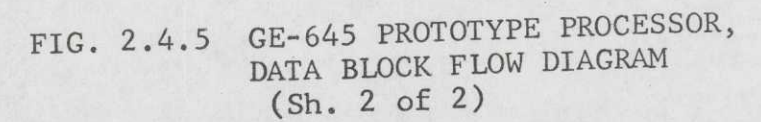
The interfaces between the Processor Module and other elements of the GE-645 Prototype System are covered in Section 5.0 of this specification.

2.4.5 PROCESSOR LOGIC ORGANIZATION

The logical arrangement of functional elements within the four functional units specified by the 645 ESS and this specification shall conform to Fig. 2.4.5. Figure 2.4.5 shows the data flow paths between the major registers, adders and switches that are necessary to perform all Processor functions. Tables listing the name, function, and format for the program accessible registers and program non-accessible registers are contained immediately following Fig. 2.4.5. The switches and logic configurations shown on Fig. 2.4.5 are not listed in the tables.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Cont. on Sh. 2-17 Sh. No. 2-16



TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

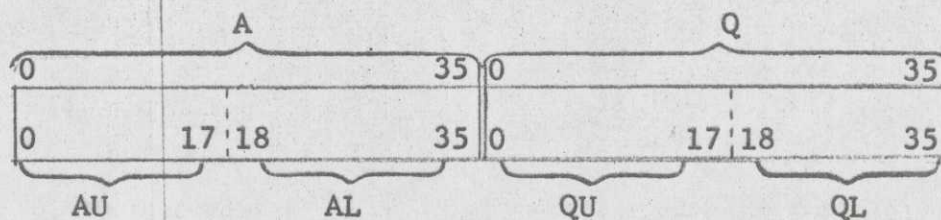
2.4.5.1 Program Accessible Registers and Formats

The registers that are accessible to the programmer via the instruction repertoire shall consist of those registers listed in paragraph 3.5.6 of the 645-ESS. These registers are also listed on Table 2.4.5.1 with their respective register formats.

Table 2.4.5.1 Program Accessible Registers and Formats

Name	Mnemonic	Bit Length	Function
1) Accumulator-Quotient Register	AQ	72	a. In floating-point operations as a mantissa register for single and double precision. b. In fixed-point operations as an operand register for double precision. c. In fixed-point operations as operands for single precision where each AQ half serves independantly of the other. The halves are then called the Accumulator (A_{0-35}) and the Quotient Register (Q_{0-35}). d. In address modification each half of A as well as Q is an index called AU(A_{0-17}), AL(A_{18-35}), QU(Q_{0-17}) and QL(Q_{18-35}).

AQ Format

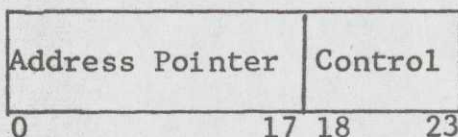


TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Table 2.4.5.1 Program Accessible Registers and Formats

Name	Mnemonic	Bit Length	Function
2) Address Base Register n (n=0,1,...,7)	ABRn	24	Contains the address pointer to a particular segment of memory and the control information required during the address appending process.

ABRn Format



Address Pointer - Consists of an 18-bit relative address consisting of a page and word number pointing to the base of a particular segment of memory.

large page - bits 0-7 specify page number; bits 8-17 specify word number.

small page - bits 4-11 specify page number; bits 12-17 specify word number.

Control -

bits 18-20 designate an ABRn ("external") linked to the "internal" ABRn designated by the instruction.

bit 21 designates that this ABR is internal ("0") or external ("1")

bit 22 designates whether this ABR may be changed in Slave mode ("1")

bit 23 unassigned.

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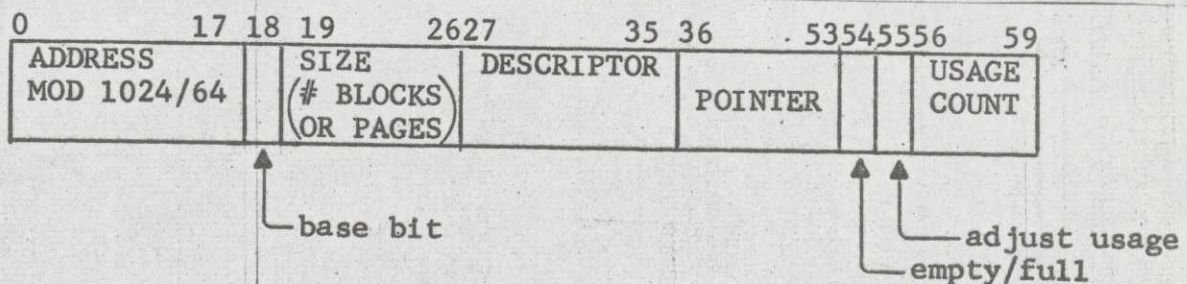
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Cont. on Sh. 2-20 Sh. No.2-19

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Name	Mnemonic	Bit Length	Function
3) Associative Memory (16 Associative Registers AR)	AM	16 registers of 60 bits	High speed memory used in appending, consisting of 16 Associative Registers (AR) of 60-bit capacity containing recently referenced segment and page locations and other related information. The Associative Memory is content addressable rather than location addressable.

AR Format (each of 16 registers)



TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3) - contd

Address -	}	An explanation of these fields for SDW, PTW and DSPTW words in the Associative Memory is contained in paragraph 2.5.5.
Size -		
Base bit -		
Descriptor Field -		

Pointer

bits 36-53 - the definition of the pointer is explained in paragraph 2.2.3 and the format is the same as ABRn 0-17.

Empty/Full

bit 54 - indicates that this register is considered empty ("0") or full ("1"). Empty means that any information contained in the respective AR is invalid and will not be considered when looking for a Segment Descriptor or Page Table Word.

Adj. Usage

bit 55 - indicates that the usage count of this register must be adjusted by the hardware.

Usage Count

bits 56-59 - indicate the usage value associated with the contents of this register, in relation to all other Associative Registers. This value is a unique number in the range 0-15.

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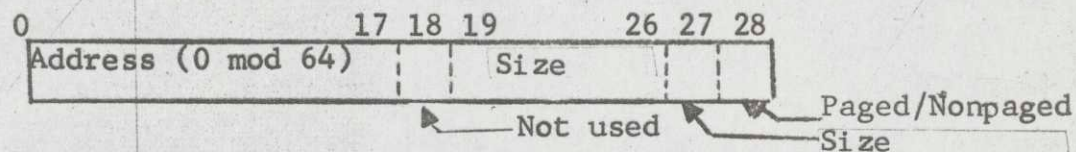
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Cont. on Sh. 2-22 Sh. No. 2-21

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Name	Mnemonic	Bit Length	Function
4) Descriptor Segment Base Register	DSBR	29	Contains the address of the descriptor segment and related control information used in the appending process.

DSBR Format

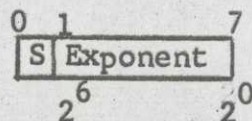


- Address -** bits 0-17 hold the base address of the segment as a modulo 64 address.
- Size** bits 19-26 a value in these positions is interpreted as the number of pages in the segment designated by bits 0-17.
- Size -** bit 27 indicates that the segment is made up of 64 word ("1") or 1024 word ("0") pages if paged; or a modulo 64 or 1024 block if non-paged.
- Page/Non-paged -** bit 28 indicates whether the segment is paged ("0") or non-paged ("1").

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Name	Mnemonic	Bit Length	Function
5) Exponent Register	E	8	The E-register supplements the AQ-register in floating-point operations, serving as the Exponent Register for the floating-point number.

E Format

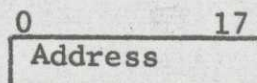


S- bit 0 indicates the sign of the exponent; plus if "0", minus if "1".

Exponent bits 1-7 contains a number from 0 to 128 representing the exponent of a floating point number residing in the AQ-register.

6) Instruction Counter	ICTC	18
------------------------	------	----

ICTC Format



When in the append mode contains the relative address in the current segment of the instruction that is currently being processed by the Control Unit. When in the absolute mode contains the absolute address.

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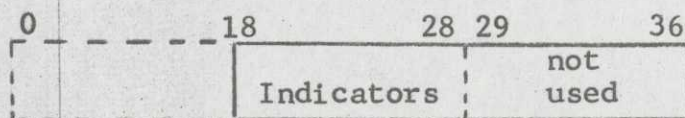
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Cont. on Sh. 2-24 Sh. No. 2-23

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Name	Mnemonic	Bit Length	Function
7) Indicator Register	IR	18	The Indicator Register is a generic term for all the program accessible "indicators" within the Processor as opposed to a large number of status "flags" defining the state of the Processor which are stored by the SCU instruction. (See SCU instruction description in Appendix A). The name Indicator Register is used where the set of indicators, listed below, appear as a source or destination of data.

IR Format



All indicators may be considered as a physical register occupying the lower half of a memory location (bits 18-28). The instructions dealing with the indicators shall assume the following bit position versus indicator function.

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Spec. No. M50EB00107

Cont. on Sh. 2-25 Sh. No. 2-24

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

7) - contd

bit 18

(Zero) - The Zero indicator is affected by instructions that change the contents of a Processor register (A,Q,AQ,Xn,IR,TR) or an adder involved in arithmetic operations and by comparison instructions. The indicator is set ON when the new contents of the affected register or adder contains all binary 0"s; otherwise the indicator is set OFF.

bit 19

(Negative)- This indicator is affected by instructions that change the contents of a Processor register (A,Q,AQ,Xn,IR,TR) or an adder involved in arithmetic operations and by comparison instructions. The indicator is set ON when the new contents of bit position 0 of this register or adder is a binary 1; otherwise it is set OFF.

bit 20 - The Carry indicator is affected by left shifts, additions, subtractions, and comparisons. It is set ON when a carry is generated out of bit position 0, otherwise it is set OFF.

bit 21 - The Overflow indicator is affected by all arithmetic instructions except add-or subtract-logical instructions or compare instructions. It is set ON when the carry into the high order bit position of the register involved does not equal the carry out.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

7) - contd

- bit 22 - This indicator is affected by arithmetic
(Exponent operations with floating-point numbers
Overflow) or with the Exponent Register, and is set ON when the exponent of the result is larger than the exponent range of +127. Since it is not automatically set to OFF otherwise, the Exponent overflow indicator reports any overflow that has happened since it was last set OFF by certain instructions (Load Indicator Register, Return, Return Double, Restore Control Unit, and Transfer on Exponent Overflow).
- bit 23 - The Exponent Underflow indicator is
(Exponent identical to the Exponent Overflow
Underflow) indicator, but responds to exponents which are less than -128.
- bit 24 - The Overflow Mask indicator can be set
(Overflow ON or OFF only by the instructions: Load
Mask) Indicators, Restore Control Unit, Return and Return Double. When the Overflow Mask indicator is ON, then the setting ON of the Overflow, Exponent Overflow, or Exponent Underflow indicators does not cause an Overflow Fault Trap to occur. When the Overflow Mask indicator is OFF, such a trap will occur. Clearing of the Overflow Mask indicator to the unmasked state does not generate a fault from a previously set Overflow or Underflow indicator, and a change in status of the Overflow Mask indicator does not affect the setting, testing, or storing of the Overflow or Underflow indicators.

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Spec. No. M50EB00107

Cont. on Sh. 2-27 Sh. No. 2-26

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

7) - contd

bit 25 - (Tally Runout) The Tally Runout indicator is affected by the Indirect then Tally address modification (except Indirect and Fault) and by Repeat, Repeat Double, and Repeat Link instructions. It is set OFF prior to executing the repeated instructions. Termination of a "Repeat" instruction because a specified terminate condition is met keeps the Tally Runout indicator OFF. Termination of a "Repeat" instruction because the tally count reaches 0 (and for Repeat Link because of a 0 link address) sets the Tally Runout indicator to ON. The Tally Runout indicator is set ON for tally equal to 0 in Indirect then Tally address modifications DI, DIC, ID, IDC, AD, SD, SC, SCR.

bit 26 - (Parity Error) The Parity Error indicator is set ON When a parity error is detected during the access of one or both words from memory. It is set OFF by Load Indicators, Return, Restore Control Unit, or Return Double instructions.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

7) - contd

bit 27 - (Parity Mask) The Parity Mask indicator can be set to ON or OFF only by the Load Indicators, Restore Control Unit, Return, and Return Double instructions. When the Parity Mask indicator is ON, the setting of the Parity Error indicator does not cause a Parity Error Fault Trap to occur; When OFF such a trap will occur. If a parity error occurs on an SDW or PTW, the Parity Error Fault Trap occurs regardless of the state of the Parity Mask indicator. Clearing of the Parity Mask indicator to the unmasked state does not generate a fault from a previously set Parity Error indicator. The status of the Parity Mask indicator does not affect the setting, or storing of the Parity Error indicator.

bit 28 - (Absolute Mode) When a "1" the Processor is in the Absolute mode of addressing and Master mode of execution. When a "0" the Processor is in Append mode of address but may be in Master or Slave mode of execution.

bits 29-35 - These bit positions are not to be used at this time.

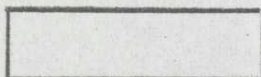
8) Index Register(n) (n=0,1,...7)

Xn 18

The Index Registers are used:
a. In fixed-point operations as operand registers for half precision.
b. In address modification as index registers.

Xn Format

0 17



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Spec. No. M50EB00107

Cont. on Sh. 2-29 Sh. No. 2-28

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>Name</u>	<u>Mnemonic</u>	<u>Bit Length</u>	<u>Function</u>
9) Procedure Base Register	PBR	18	Contains the address (0 modulo 64) of the base of the procedure segment currently in execution, when not in Absolute mode.

PBR Format

0 17

Address Pointer

Address Pointer - same as previously described for ABRn.

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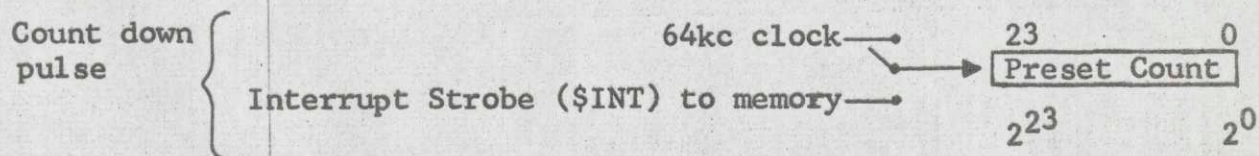
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Cont. on Sh.2-30 Sh. No.2-29

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

	<u>Name</u>	<u>Mnemonic</u>	<u>Bit Length</u>	<u>Function</u>
10)	Timer Register	TR	24	Provides the capability for providing a program interrupt at the end of a variable interval. Maximum total elapsed time may be set to approximately four minutes. A manually operated switch is also provided which allows the Timer Register to be counted down by a pulse which requests memory cycles from the memory, or, from an internal 64 kc clock (15.625 microsecond intervals). Whenever the Timer Register contents reach zero a Timer Runout Fault Trap occurs if the Processor is in Slave mode. If the Processor is in Master mode no fault occurs until a return to Slave mode but decrementation of the Timer Register continues beyond zero. (Decrementation starts again from a maximum count).

TR Format



TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

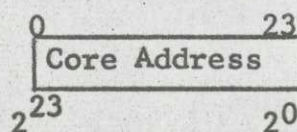
2.4.5.2 Program Nonaccessible Registers and Formats

The terminology "program nonaccessible registers" as it is used in this specification includes all major registers and adders that are not accessible directly through the instruction repertoire. These registers and adders shall be implemented to support the functions of the program accessible registers and the individual instructions. These registers are listed in Table 2.4.5.2 with the formats, where necessary, to show the required implementation.

Table 2.4.5.2 Program Nonaccessible Registers

Name	Mnemonic	Bit Length	Function
1) Address Register	ADR	24	Contains the absolute address when making memory accesses

ADR Format



Core address - consists of a 24-bit address representing a memory location. The three bits above the bit which defines the memory size are to be used by the memory interlace logic to determine which processor port shall be requested when memories are connected to more than one processor port (See appendix B of the 645 ESS for details.)

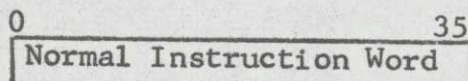
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Spec. No. M50EB00107
 Cont. on Sh. 2-32 Sh. No. 2-31

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

<u>Name</u>	<u>Mnemonic</u>	<u>Bit Length</u>	<u>Function</u>
2) C-register	C	36	The C-register contains the odd instruction word being processed by the Control Unit.

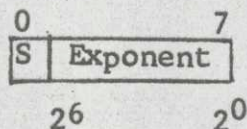
C Format



The interpretation of the fields in the C-register are explained in paragraph 2.5.4.

3) D-register	D	8
---------------	---	---

D Format



Used to hold the exponent of the operand from memory in floating-point operations.

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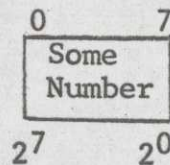
Spec. No. M50EB00107

Cont. on Sh. 2-34 Sh. No. 2-33

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

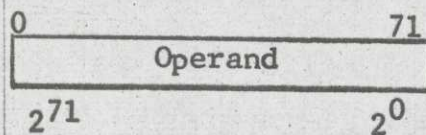
<u>Name</u>	<u>Mnemonic</u>	<u>Bit Length</u>	<u>Function</u>
7) G-Register	G	8	Contains the number of shifts for shifts, normalization and aligning, and the number of general cycles to be done on multicycle arithmetic operations.

G Format



8) H-Register	H	72	Used as a buffer register to hold one of the operands that are presented to the main adder (S-adder).
---------------	---	----	---

H Format



9) I-Register	I	72	Used as a buffer to hold the next even (I_{0-35}) -odd (I_{36-71}) instruction pair to be processed by the Control Unit allowing the Control Unit to contain up to four instructions at one time.
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Spec. No. M50EB00107

Cont. on Sh. 2-35 Sh. No. 2-34

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

<u>Name</u>	<u>Mnemonic</u>	<u>Bit Length</u>	<u>Function</u>
<u>I Format</u>			
		0 35 36 71 Even instruction Odd instruction	
			The interpretation of the fields for the even or odd instruction is the same as for the Y- and C-register and is defined in paragraph 2.5.4.
10) Instruction Counter A	ICTA	18	When in the append mode contains the relative address in the current segment of the instruction being executed by the Operations Unit: when in the absolute mode contains the absolute address.
	<u>ICTA Format</u>		
		0 17 Instruction address 2¹⁷ 2⁰	
11) Instruction Counter A'	ICTA'	18	Used as a buffer for the ICTA-register for fault correction purposes.
	<u>ICTA' Format</u>		
			Format is the same as ICTA
12) Instruction Counter B	ICTB	18	When in the append mode contains the relative address in the current segment of the instructions contained in the I-register; when in the absolute mode contains the absolute address.
	<u>ICTB Format</u>		
			Format is the same as ICTA.

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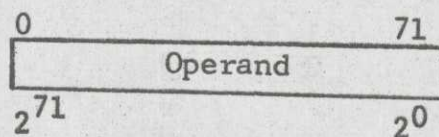
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Cont. on Sh. 2-36 Sh. No. 2-35

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>Name</u>	<u>Mnemonic</u>	<u>Bit Length</u>	<u>Function</u>
13) M-Register	M	72	Used as an intermediate register to buffer operands coming in from memory to the Operations Unit. Also used to hold the multiplier on multiply operations.

M Format

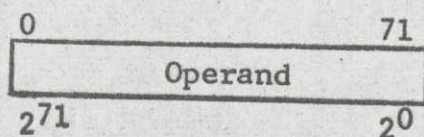


14) N-Register

N 72

Used as a buffer register to hold the second of the operands that are presented to the main adder (S-adder) in the Operations Unit.

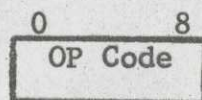
N Format



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 GE-645 PROTOTYPE PROCESSOR

<u>Name</u>	<u>Mnemonic</u>	<u>Bit Length</u>	<u>Function</u>
15) RE-Register	RE	9	Used as a buffer for the operation code of the even instruction that is to be sent to the Operations Unit.

RE Format



OP Code - is the 9-bit octal operation code contained in the instruction word to be executed.

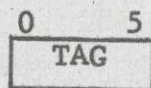
16) RO-Register	RO	9	Used as a buffer for the operation code of the odd instruction that is to be sent to the Operations Unit.
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RO Format

Same as RE format

17) Tag Register	CT	6	Contains the tag portion of the instruction when IR or IT type address modification is specified by the instruction word. (See paragraph 2.5.4 for definition of instruction word.)
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CT Format

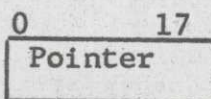


Tag - contains the tag field of the instruction or indirect word (bits 30-35) for IR or IT address modification.

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

<u>Name</u>	<u>Mnemonic</u>	<u>Bit Length</u>	<u>Function</u>
18) Temporary Base Register	TBR	18	Contains the address pointer used to link addresses during the address appending process.

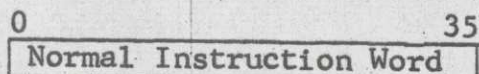
TBR Format



Pointer - The pointer is an 18 bit address value which points to a segment or page of a segment in memory, and is used in the address appending process. A further definition of pointer is contained in paragraph 2.5.3.

19) Y-Register	Y	36	Contains the even instruction of the even-odd pair of instructions that the Control Unit is currently processing.
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Y Format



The interpretation of the fields in the Y-register are the same as the C-register and are contained in paragraph 2.5.4.

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Spec. No. M50EB00107

Cont. on Sh. 2-39 Sh. No. 2-38

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

<u>Name</u>	<u>Mnemonic</u>	<u>Bit Length</u>	<u>Function</u>
20) Z 1-register	Z1	5	Contains a code (developed from the operation code) which indicates what Processor registers are in use in the execution of the instruction which preceded the one the Control Unit is now working on.
<u>Z1 Format</u> 04 Code Code - a five bit code is to be developed from the operation code to designate the affected registers.			
21) Z 2-register	Z2	5	Same as the Z 1-register but for the instruction which preceded by two the one the Control Unit is now working on.
<u>Z2 Format</u> Same as Z1.			
22) ESTR-register ESTR		4	Contains the segment tag (bits 0-2 of the instruction word) and bit 29 of the instruction word contained in the even instruction register, (Unless changed by an ITB modifier to a new tag). Bits 0-2 designate an ABR for appending purposes.
<u>ESTR Format</u> 023 bit 29 of even instruction word bits 0-2 of even instruction word			
23) OSTR-register OSTR		4	Same as ESTR, but for the odd instruction word.

Spec. No. M50EB00107

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

NOTE

Diagram illustrating a 1D lattice with n sites. The top horizontal line is labeled 0 at the left end and $n-1$ at the right end. The bottom horizontal line is labeled 2^{n-1} at the left end and 2^0 at the right end.

24)	BS-adder	18	Used to add the internal base during the appending process. The output of the BS-adder is the effective address (EA) of the operand which is to be requested from memory. It is presented to the Relocation (RS) Adder in the appending Unit.
25)	ES-adder	10	Used as the Exponent Adder in floating-point operation
26)	RS-adder	18	Used to compute the final most significant 18-bits of the address that is presented to the Address Register in forming the 24-bit absolute address to access core memory.
27)	S-adder	72	Used as the main Processor Adder for fixed-and floating-point additions, subtractions, multiplications, and divisions.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

	<u>Name</u>	<u>Bit Length</u>	<u>Function</u>
28)	US-adders	4	Used to adjust the usage value of each register of the Associative Memory.
29)	YS-adder	18	Used to compute the preliminary address of instructions and operands, with any specified address modification, that is presented to the BS-adder.

2.5 INFORMATION REPRESENTATION

The GE-645 Prototype Processor shall be fundamentally organized to deal with 36-bit groupings of information. In addition, 6-, 9-, and 18-bit groups plus 72-bit double precision groups shall be manipulated via the instruction set. These bit groupings are used by the hardware and software to represent a variety of forms of information. All notation used throughout the Processor is in binary. The way information is represented for instruction, indirect, appending and Associative Memory words is included in these paragraphs.

2.5.1 NUMBER SYSTEM

With the binary system of notation used throughout the Processor, many of the instructions (mainly additions, subtractions, and comparisons) can be used in two ways: either operands and results are regarded as signed binary numbers in the 2's complement form (the "arithmetic" case), or they are regarded as unsigned positive binary numbers (the "logic" case). Hardware actions within the Processor are the same in either case; interpretation of the data by the programmer is the only difference. The Zero and Negative indicators facilitate the general interpretation of the results in the arithmetic case; the Zero and Carry indicators in the logic case. In the instruction set are "Add Logic" instructions which particularly facilitate arithmetic of the logic type with half-word, single-word, and double-word precision.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.5.1 - contd

Subtractions are carried out internally by adding the 2's complement of the subtrahend.

NOTE

When the subtrahend is zero, the algorithm for forming the 2's complement is still carried out. Thus, each bit of the subtrahend is complemented and a "1" is added into the least-significant bit position of the parallel adder yielding zeros.

It is a characteristic feature of the 2's complement representation that a "no borrow" condition in the case of true subtraction corresponds to a "carry" condition in the case of addition of the 2's complement, and vice versa.

A statement on the assumed location of the binary point has significance only for multiplications and divisions. These two operations are implemented for integer arithmetic as well as for fractional arithmetic with numbers in 2's complement form. "Integer" meaning that the position of the binary point may be assumed to the right of the least-significant bit position (that is, to the right of bit position 35 or 71, depending on the precision of the respective number) and "fractional" meaning that the position of the binary point may be assumed to the left of the most-significant bit position (that is, between the bit positions 0 and 1).

2.5.2 PROCESSOR MACHINE WORD

The machine word consists of 36 bits arranged as shown on Fig. 2.5.2. Numbering of bit positions and character positions within the machine word and double words, in cases where 72 bits are involved, increases in the direction of conventional reading and writing: from the most- to the least-significant digit of a number, and from left to right in conventional alphanumeric text.

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Spec. No. M50EB00107

Cont. on Sh. 2-43 Sh. No. 2-42

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

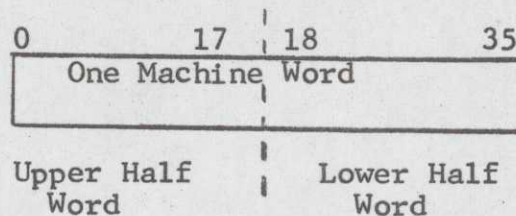


Fig. 2.5.2 The Machine Word

Data transfers between the Processor and memory are word orientated: 36 bits are transferred at a time for single-precision data and two successive 36-bit word transfers for double-precision data. Parity on words transferred to, or read from the memory module are handled completely within that module. The Processor is notified only if a parity error exists.

The Processor has features for transferring and processing pairs of words. In transferring a pair of words to or from memory, a pair of memory locations is accessed; these addresses are an even and the next-higher odd number as shown in Fig. 2.5.2a.

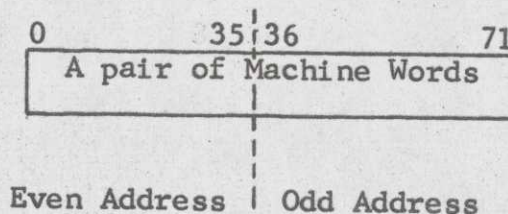


Fig. 2.5.2a the Pair of Machine Words

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 GE-645 PROTOTYPE PROCESSOR

In addressing such a pair of memory locations in an instruction that is intended for handling pairs of machine words, either of the two addresses may be used as the absolute address (Y) except as noted under the instruction descriptions. Thus, if Y is even, the pair of locations (Y, Y+1) is accessed. If Y is odd, the pair of locations (Y-1, Y) is accessed. The term "Y-pair" is used for each such pair of addresses.

2.5.3 REPRESENTATION OF DATA

Data is represented in two forms: alphanumeric or numeric. Both forms may be handled by the hardware as indicated by the instruction repertoire.

2.5.3.1 Alphanumeric

Alphanumeric data are represented by 6- or 9-bit characters. A machine word contains either six or four characters as shown on Fig. 2.5.3.1.

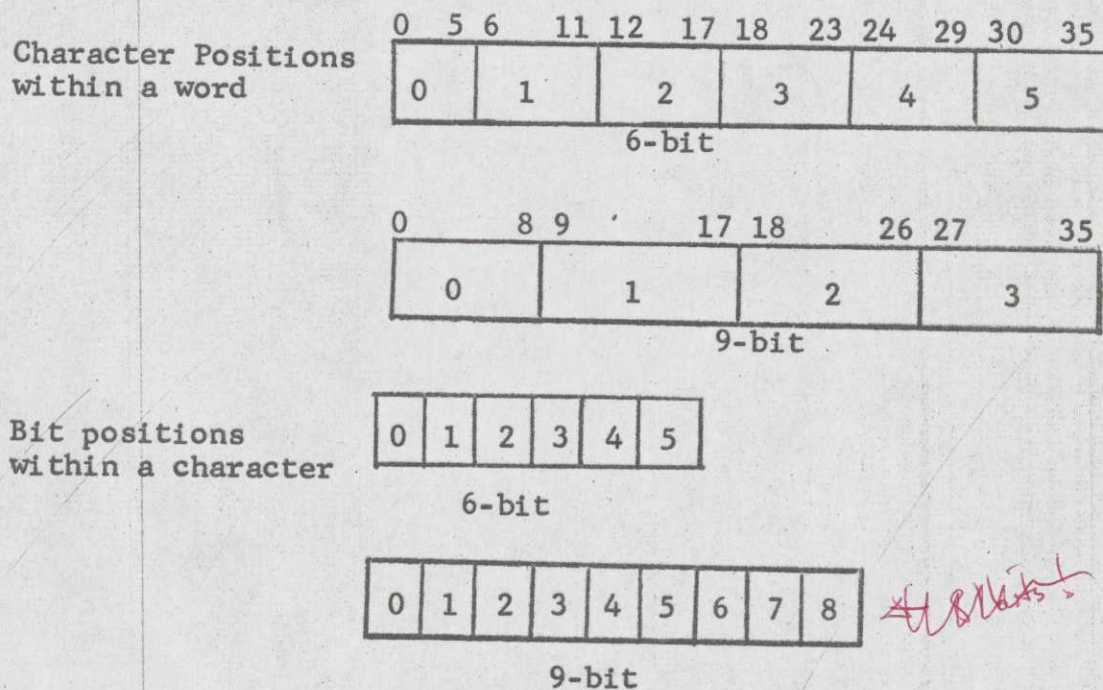


Fig. 2.5.3.1 Character Positions Within the Machine Word

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 GE-645 PROTOTYPE PROCESSOR

The character set used to code programs is the Computer Equipment Department Standard Character Set, which is readily convertible to and from the ASCII character set. It is expected that the Operating Supervisor (Multics - 645/I) shall use the ASCII character set.

2.5.3.2 Numeric

Numeric data is represented in two forms; binary fixed-point, or binary floating-point. Decimal data is handled by software.

Binary Fixed-Point Numbers -- The instruction set comprises instructions for binary fixed-point arithmetic with half-word, single-word, and double-word precision as shown on Fig. 2.5.3.2.

PRECISION

REPRESENTATION

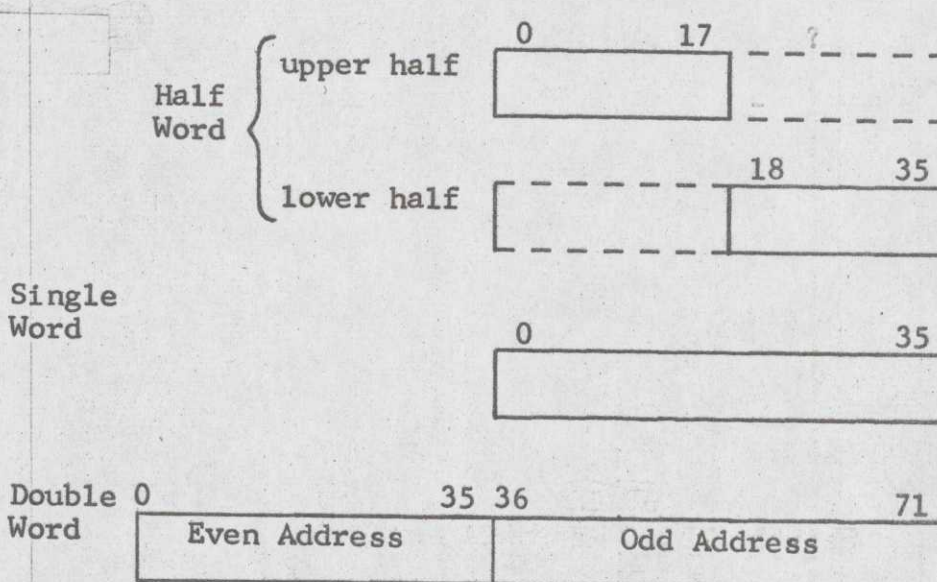


Fig. 2.5.3.2 Representation of Half-word, Single-Word, and Double-word Precision, Numeric Formats.

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GE-645 PROTOTYPE PROCESSOR

Instructions are divided into two groups according to the way in which the operand is interpreted by the programmer: the "logic" group and the "algebraic" group.

For the "logic" group, operands and results are regarded as unsigned, positive binary numbers. In the case of addition and subtraction, the occurrence of any overflow is reflected by the carry out of the most-significant (leftmost) bit position.

- 1) Addition - If the carry out of the leftmost bit position equals 1, then the result is above the range.
- 2) Subtraction - If the carry out of the leftmost bit position equals 0, then the result is below the range.

In the case of comparisons, the Zero and Carry indicators show the relation.

For the "algebraic" group, operands and results are regarded as signed, binary numbers, the leftmost bit being used as a sign bit, (a 0 being plus and 1 minus). When the sign is positive all the bits represent the absolute value of the number; and when the sign is negative, they represent the 2's complement of the absolute value of the number.

In the case of addition and subtraction the occurrence of an overflow is reflected by the carries into and out of the leftmost bit position (the sign position). If the carry into the leftmost bit position does not equal the carry out of that position, then overflow has occurred. If overflow has been detected and if the sign bit equals 0, the resultant is below range; if with overflow, the sign bit equals 1, the resultant is above range.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

An explicit statement about the assumed location of the binary point is necessary only for multiplication and division. When performing addition, subtraction, and comparison it is sufficient to assume that the binary points are "lined up". In the GE-645 Prototype Processor, multiplication and division are implemented in two forms for 2's complement numbers: integer and fractional.

- 1) In integer arithmetic, the location of the binary point is assumed to the right of the least-significant bit position, that is, depending on the precision, to the right of bit position 35 or 71. The general representation of a fixed-point integer is then:

$$- a_n 2^n + a_{n-1} 2^{n-1} + a_{n-2} 2^{n-2} + \dots + a_1 2^1 + a_0 2^0$$

^
binary point

where a_n is the sign bit.

- 2) In fractional arithmetic, the location of the binary point is assumed to the left of the most-significant bit position, that is, to the left of bit position 1. The general representation of a fixed-point fraction is then:

$$- a_0 2^0 + a_1 2^{-1} + a_2 2^{-2} + \dots + a_{n-1} 2^{-(n-1)} + a_n 2^{-n}$$

^
binary point

The number ranges for the various cases of interpretation, precision, and arithmetic are listed in Table 2.5.3.2.

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Table 2.5.3.2 Ranges of Fixed-Point Numbers

Inter-pretation	Arithmetic	Precision		
		Half-Word (Xn, Y ₀₋₁₇)	Single-Word (A,Q,Y)	Double-Word (AQ,Y-pair)
Algebraic	Integral	$-2^{17} \leq N \leq (2^{17}-1)$	$-2^{35} \leq N \leq (2^{35}-1)$	$-2^{71} \leq N \leq (2^{71}-1)$
	Fractional	$-1 \leq N \leq (1-2^{-17})$	$-1 \leq N \leq (1-2^{-35})$	$-1 \leq N \leq (1-2^{-71})$
Logic	Integral	$0 \leq N \leq (2^{18}-1)$	$0 \leq N \leq (2^{36}-1)$	$0 \leq N \leq (2^{72}-1)$
	Fractional	$0 \leq N \leq (1-2^{-18})$	$0 \leq N \leq (1-2^{-36})$	$0 \leq N \leq (1-2^{-72})$

Binary Floating-Point Numbers -- The instruction set contains instructions for binary floating-point arithmetic with numbers of single-word and double-word precision (Fig. 2.5.3.2a). The upper 8 bits represent the integral exponent E in the 2's complement form, and the lower 28 or 64 bits represent the fractional mantissa M in 2's complement form. The notation for a floating-point number Z is:

$$Z = M_2 \times 2^E$$

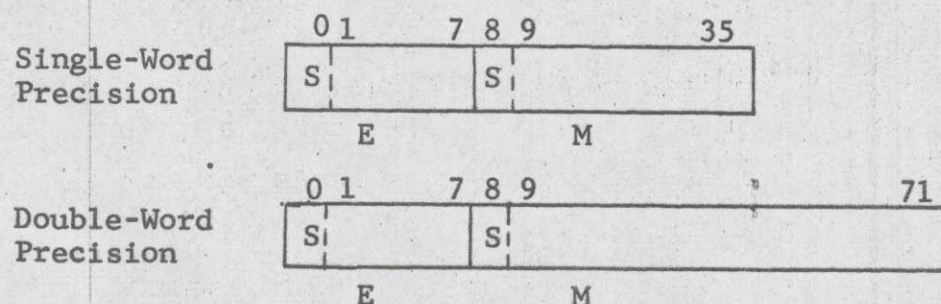


Fig. 2.5.3.2a Representation of Floating-Point Numbers

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 2-49 Sh. No. 2-48

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Before doing floating-point additions or subtractions, the Processor shall align the number which has the smaller positive exponent. To maintain accuracy, the lowest permissible exponent of -128 together with the mantissa equal to 0.000 shall be defined as the machine representation of the number zero (which has no unique floating-point representation. Whenever a floating-point operation yields a resultant untruncated machine mantissa equal to zero (71 bits plus sign because of extended precision), the exponent is automatically set to -128. The general representation of the exponent for single and double precision is:

$$- e_7 2^7 + e_6 2^6 + \dots + e_1 2^1 + e_0 2^0$$

where e_7 is the sign.

The general representations of single- and double-precision mantissas are:

$$\begin{aligned} \text{Single Precision: } & - m_0 2^0 + m_1 2^{-1} + m_2 2^{-2} + \dots \\ & + m_{26} 2^{-26} + m_{27} 2^{-27} \end{aligned}$$

$$\begin{aligned} \text{Double Precision: } & - m_0 2^0 + m_1 2^{-1} + m_2 2^{-2} + \dots \\ & + m_{62} 2^{-62} + m_{63} 2^{-63} \end{aligned}$$

where m_0 is the sign in both cases.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.2=50 Sh. No.2-49

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Normalized Floating-Point Numers -- For normalized floating-point numbers, the binary point is placed at the most-significant bit of the mantissa (to the right of the sign bit). Numbers are normalized by shifting the mantissa (and correspondingly adjusting the exponent) until no leading zeros are present in the mantissa for positive numbers, or until no leading ones are present for the negative numbers. Zeros fill in the vacated bit positions. With the exception of the number zero (represented as 0×2^{-128}), all normalized floating-point numbers will contain a binary 1 in the most-significant bit position for positive numbers and a binary 0 in the most-significant bit position for negative numbers. Some examples are:

Unnormalized positive number	(0 0001101) $\times 2^7$
	S
Same number normalized	(0 1101000) $\times 2^4$
	S
Unnormalized negative number	(1 11010111) $\times 2^{-4}$
	S
Same number normalized	(1 01011100) $\times 2^{-6}$
	S

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 2-51 Sh. No. 2-50

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

The number ranges resulting from the various cases of precision, normalization, and sign are listed in Table 2.5.3.2a.

Table 2.5.3.2a Ranges of Floating-Point Numbers

	Sign	Single Precision	Double Precision
	Positive	$2^{-129} \leq N \leq (1-2^{-27})2^{127}$	$2^{-129} \leq N \leq (1-2^{-63})2^{127}$
Normalized	Negative	$-(1+2^{-26})2^{-129} \geq N \geq -2^{127}$	$-(1+2^{-62})2^{-129} \geq N \geq -2^{127}$
Unnormalized	Positive	$2^{-155} \leq N \leq (1-2^{-27})2^{127}$	$2^{-191} \leq N \leq (1-2^{-63})2^{127}$
	Negative	$-2^{-155} \geq N \geq -2^{127}$	$-2^{-191} \geq N \geq -2^{127}$

NOTE: The floating-point number zero is not included in the table.

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

2.5.4 REPRESENTATION OF INSTRUCTION, INDIRECT, AND INDIRECT THEN TALLY WORDS

All machine instructions except the "Repeat" instructions have the same general format as shown in Fig. 2.5.4. The "repeats" are handled differently and are covered in detail under the specific instructions description. Indirect words have the same general format as the instruction words (except for Indirect then Tally (IT) modification) but the fields are used somewhat differently.

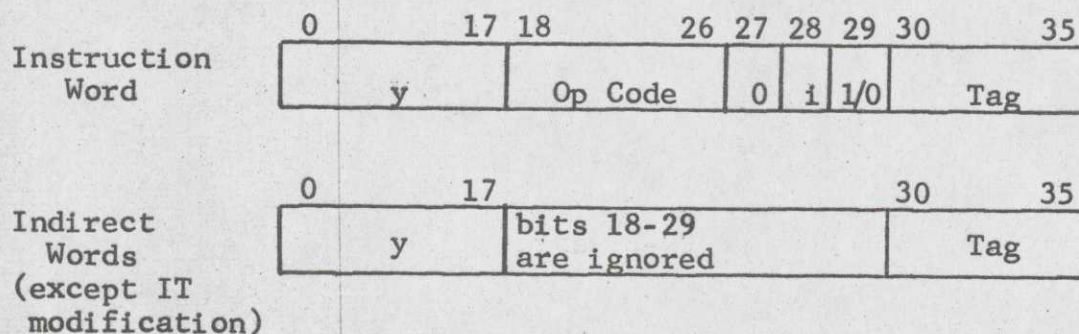


Fig. 2.5.4 Instruction and Indirect Word Format
 (except for IT modification)

Specific fields within the word are defined as follows:

y = the address field; also used in some cases to augment the Operation Code as in shift operations where it specifies the number of shifts, or in some address modifications where it is the operand.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Op Code = the Operation Code, usually stated in the form of a 3-digit octal number.

0 = no function at this time; however, bit 27 must be zero for compatability with other 600-line Processors.

1 = the interrupt inhibit bit.

1/0 = the bit which denotes whether y should be interpreted as a normal address or as a segment tag (y_{0-2}) and signed 15-bit quantity (y_{3-17}) which denotes a specific Address Base Register for Address Appending.

Tag = the tag field, generally used to control the address modification.

Tag Field

Before the operation of an instruction is carried out, an address modification procedure generally takes place as directed by the tag field of the instruction and possibly of indirect words. Only the repeat mode instructions do not provide for an address modification.

The tag field (Fig. 2.5.4a) consists of two parts, t_m and t_d , that are located within the instruction word as follows:

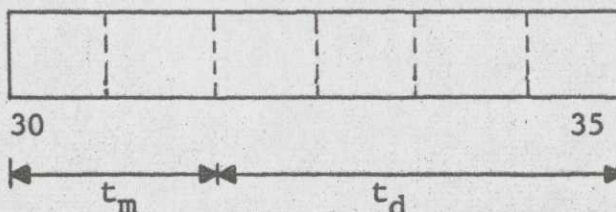


Fig. 2.5.4a Tag Field of Instruction and/or Indirect Word

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GE-645 PROTOTYPE PROCESSOR

where

t_m specifies one of the four possible modification types: Register (R), Register then Indirect (RI), Indirect then Register (IR), and Indirect then Tally (IT).

t_d specifies further the action for each modification type:

- 1) In the case of $t_m = R, RI, \text{ or } IR$; t_d is called the register designator and generally specifies the register to be used in indexing.
- 2) In the case of $t_m = IT$; t_d is called the tally designator and specifies the tallying in detail.

Tables 2.6.1; 2.6.1a and 2.6.1b list the symbolic and binary codes and the different types of modification.

Tally Designators for IT Modification

The modification type IT consists of a substitution and the use of the indirect word of Fig. 2.5.4b as specified by the t_d of the designator (except for ITB or ITS).

0	17 18	29 30	35
y	Tally	Tag	

Fig. 2.5.4b Indirect Word for IT Modifications
(except ITB or ITS)

Where

y = address field
Tally = tally field
Tag = tag field

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Depending on the tally designator of the previous instruction or indirect word, the tag field is interpreted in one of three ways as shown by Fig. 2.5.4c.

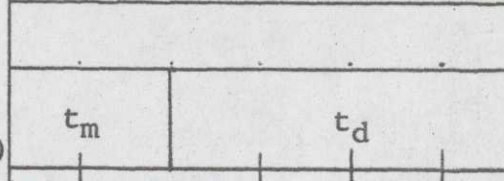
Tally Designator

Tag Field

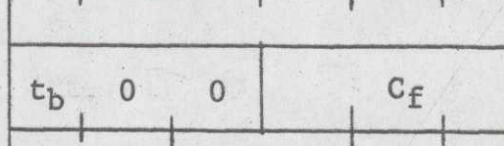
I,DI,ID,F,F2,F3

Ignored in indirect word,
 specified in t_d of previous
 instruction or indirect word

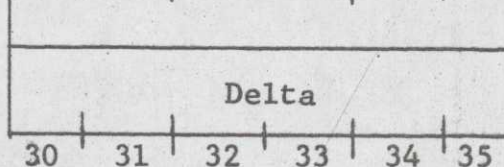
DIC,IDC,ITB,ITS (ITS
 and ITB require both
 t_m , and t_d for identification. See Fig. 2.5.4d)



CI,SC, SCR



AD,SD



30 31 32 33 34 35

Fig. 2.5.4c Tag Format of Indirect Word for IT
 Modifications (Except ITB and ITS)

where

t_m = modifier
 t_d = designator
 t_b = character size (0 = 6 bit, 1 = 9 bit)
 Delta = Delta Field
 C_f = character field

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

IT Type ITB and ITS Modification

The ITB and ITS modifications are treated somewhat differently than the normal IT modifications. The Tally Designator (t_d) for IT modification which specifies ITB and ITS will only be recognized when specified by t_m , t_d of the tag field of an even indirect word that resulted from RI or IR modification. Whenever RI and IR modification is specified and EA is an even address, an even-odd pair of indirect words are pulled from memory in anticipation of an ITB or ITS modifier. The even-odd pair word format as represented in memory is as shown in Fig. 2.5.4d. The odd word of the pair is a normal indirect word relative to the base specified by the even word.

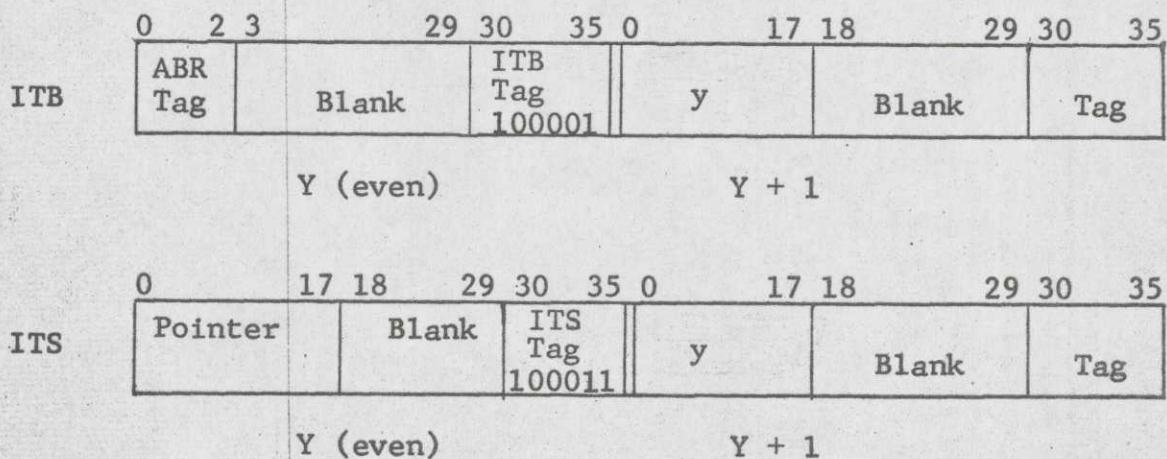


Fig. 2.5.4d ITB and ITS Word Formats in Memory

A discussion and explanation of the different types of address modification in greater detail is contained in paragraph 2.6.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.5.5 APPENDING WORDS

The address appending process uses a number of control words to link addresses and control access to segments and pages of segments (for example, Segment Descriptor Word (SDW), Page Table Word (PTW), Descriptor Segment Page Table Word (DSPTW)). Requirements for these words are spelled out in the 645 ESS, paragraph 3.5.8 and paragraph 2.2 of this specification. Representation of the appending words in core memory are shown in Figs. 2.5.5 and 2.5.5a. Representation of the appending words in Associative Memory is shown in Figs. 2.5.6a, and 2.5.6b. The SAM and ZAM instructions store the associative memory SDW, or PTW.

Segment Descriptor Word in Core Memory

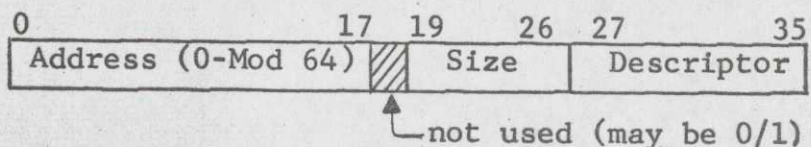


Fig. 2.5.5 SDW Word Format in Core Memory

Where: Address - bits 0-17 contain the base address of the segment being accessed or of the segment page table

Size - bits 19-26 contain the total number of pages in the segment if paged; or the number of blocks if not paged.

Descriptor - bit 27 indicates block or page size; 64/1024 ("1"/"0" respectively)

bit 28 indicates segment paged or nonpaged ("0"/"1" respectively)

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.5.5 - contd

bit 29 not used.

bit 30 (write permit) if "1" this page may be written into in Slave mode.

bit 31 (Master access) if "0" indicates access in Master mode only. If "1" access in Master or Slave

bit 32 used when bits 33-35 indicate a Directed fault

bits 33-35 (Class)

000 - Directed Fault (see paragraph 2.9; bits 30-32 contain the fault code)

001 - Data,- no execution

011 - Procedure-Execute Only

010 - Procedure-Slave (may contain data)

100 - Procedure-Master (may contain data)

Page Table Word (PTW) in Core Memory

0	17	25	35
Address (0-Mod 64/1024)	not used	Descriptor	

Fig. 2.5.5a PTW Format in Core Memory

where:

Address - bits 0-17 contain the base address of the page being accessed.

Descriptor - bit 25 (used bit) if "1", the page has been referenced.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.5.5 - contd

bit 26 (written bit) if "1"
the page has been written
into.

bits 27-29 not used

bit 30 (write permit bit) if
"1" this page may be written
into in Slave mode.

bit 31 (Master Access) if
"0" this page may be accessed
in Master mode only. If "1"
access in Master or Slave.

bit 32 used when bits
33-35 indicate a directed
fault.

bits 33-35 (Class)

- 000 - Directed Fault (See
paragraph 2.9; bits 30-32
contain the fault code)
- 001 - Data - no execution
- 011 - Procedure-Execute
only
- 010 - Procedure-Slave (may
contain data)
- 100 - Procedure-Master (may
contain data)

Descriptor Segment Page Table Word (DSPTW)- same format as the
PTW.

2.5.6 ASSOCIATIVE MEMORY WORD

The Associative Memory shall contain 16 Associative
Registers, the contents of which shall be interpreted
as shown in Fig. 2.5.6.

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

2.5.6 - contd

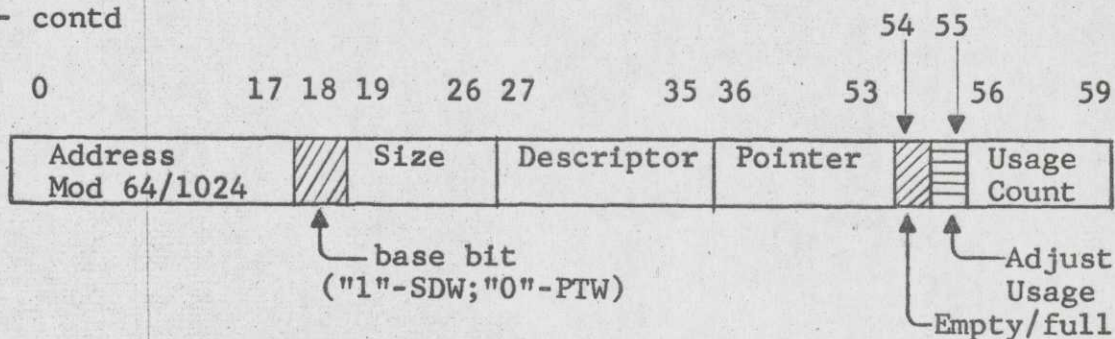


Fig. 2.5.6 Associative Memory Word Format

Where:

- | | |
|-------------------|--|
| Address | - The address is for the following:

1) If A M word is for a SDW then address is for the base of Segment if nonpaged; or the base of the Segment Page Table if paged.

2) If A M word is for PTW then address is for base of page. |
| Size | - Total number of pages in segment if paged; or number of blocks if not paged. |
| Base Bit | - If a "1", Associative Register contains an SDW; if a "0", contains a PTW. |
| Descriptor | - Same as for SDW if the Associative Register contains an SDW. If Associative Register contains a PTW then Descriptor contains the most restrictive of the SDW and PTW Descriptors. |
| Pointer | - <u>bits 36-53</u> an 18 bit address that points to the base of a segment or to a page of a segment; normally the address content of one of the eight Address Base Registers (ABRO-7) or Procedure Base Register (PBR). |

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 PHOENIX, ARIZONA

Spec. No. M50EE00107

Cont. on Sh. 2-61 Sh. No. 2-60

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

2.5.6 - contd

Empty/Full

- bit 54 when a "1" indicates that the Associative Register has valid information.

Adjust Usage

- bit 55 indicates that the usage count must be adjusted by the hardware.

Usage Count

- bits 56-59 contains a unique number in the range 0-15 which is the usage value of this particular Associative Register. This number shall be changed automatically by the hardware as new words are brought into the Associative Memory. New Words shall contain a usage count of 15 and shall replace the word with a usage count of 0. The register that is most active shall have a usage count of 15; the least active a count of 0.

The format of SDW or PTW words in Associative Memory is contained in Figs. 2.5.6a and 2.5.6b.

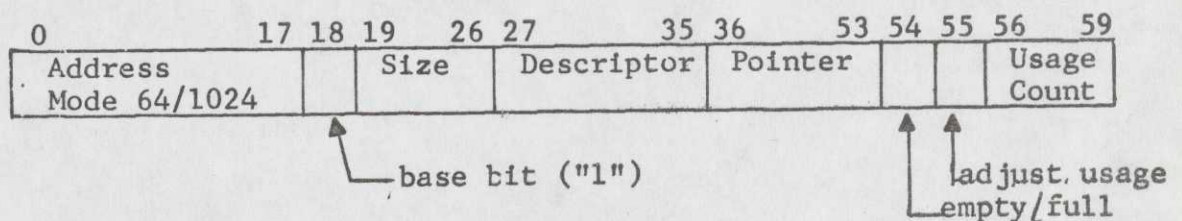


Fig. 2.5.6a SDW in Associative Memory

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

2.5.6 - contd

Address	- Same as SDW (Fig. 2.5.5)
Base Bit	- Contains a logical "1".
Size	- Same as SDW (Fig. 2.5.5)
Descriptor	- Same as SDW (Fig. 2.5.5)
Pointer	-
Empty/full	-
Adjust Usage	- Same as Associative Memory Word (Fig. 2.5.6)
Usage Count	-

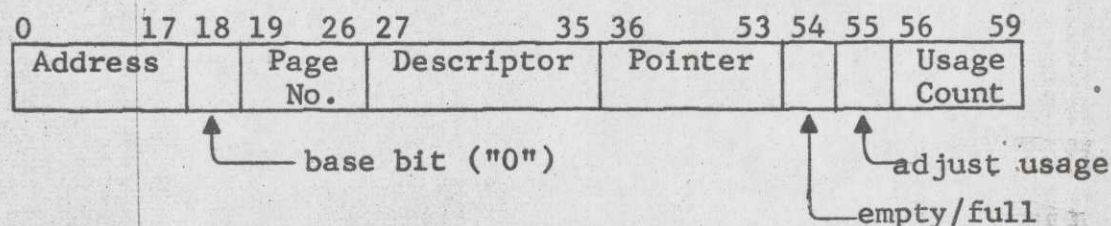


Fig. 2.5.6b PTW in Associative Memory

Address	- Same as PTW (Fig. 2.5.5a)
Base Bit	- Contains a logical "0"
Page No.	- The page number of the PTW from the effective address formed by the Control Unit.
Descriptor	- <u>bit 27</u> page size from the associated SDW ₂₇ ; 64/1024 ("1"/"0" respectively). bit 28 paged or nonpaged bit from SDW ₂₈ ("0"/"1" respectively). For a PTW this will always be a "0".

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 2-63 Sh. No. 2-62

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.5.6 - contd

bit 29 written bit from PTW.
If "1" this page has been
written into.

bits 30-35 combined with bits
30-35 of SDW to reflect the most
restrictive of the access and
class control bits. (Fig. 2.5.5,
2.5.5a)

Pointer
Empty/Full
Adjust usage
Usage Count

bits 36-59
Same as Associative Memory
Word (Figure 2.5.6).

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.6 ADDRESS MODIFICATION FOR OPERANDS

Prior to any memory access for an operand, or indirect word, two major address preparation phases shall be completed:

- 1) Address modification (if specified by the instruction or indirect word) to form the Effective Address (EA) for the operand.
- 2) Address appending to further process the 18-bit effective address to form a 24-bit absolute address used to access memory. When the Processor is addressing in the Absolute mode, the 18-bit effective address is used to access memory, unless bit 29 of the instruction word is set to "1," indicating that appending is to be performed.

Address modification is discussed in the following paragraphs. Address appending is discussed separately in paragraph 2.7. Representation of instruction, indirect and indirect then tally word formats, and how the various fields of these words are interpreted was explained in paragraph 2.5.4. The following discussion assumes familiarity with the various formats.

2.6.1 MODIFICATION TYPES

The GE-645 shall have four distinct types of address modifications designated R, RI, IR and IT. Table 2.6.1 briefly explains each type.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 2-65 Sh. No. 2-64

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 2.6.1 Types of Address Modification

T_m of Tag Field (bits 30-31)	Modification Type
00(R)	<u>Register</u> Indexing according to t_d as register designator and termination of the address modification procedure.
01(RI)	<u>Register then Indirect</u> Indexing according to t_d as register designator, then substitution and continuation of the modification procedure as directed by the tag field of this indirect word.
11(IR)	<u>Indirect then Register</u> Saving of t_d as final register designator, the substitution and continuation of the modification procedure as directed by the tag field of this indirect word.
10(IT)	<u>Indirect then Tally</u> Substitution, then use of this indirect word according to t_d as tally designator (or t_m , t_d for ITS, ITB).

Additional categories of modification for each general type shall be as shown in Table 2.6.1a and 2.6.1b. Note that for R, RI and IR modification, bits 32-35 are called the Register Designators and may specify further action. Namely, that y is to be used as a direct operand (DU, DL) and not as the address of an operand, or that nothing (N) takes place at all.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

NOTE

The Register Designators DU,DL are not recognized for RI or IR modification when specified by the instruction or indirect word. If DU, DL is specified by t_d of the instruction or indirect word for RI, or IR, then an indirect word fetch will be accomplished. (See the flow chart of 2.6.2 to clarify this point.)

Table 2.6.1a R, RI, and IR Register Designators

Register Designator (td of Tag)		Action*	
Symbolic	bits 32-35		
N	0000	y	replaces EA
X0	1000	$y+C(Xn)$	replaces EA
X1	1001		
.	.		
.	.		
X7	1111		
AU	0001	$y+C(A)_{0-17}$	replaces EA
AL	0101	$y+C(A)_{18-35}$	replaces EA
QU	0010	$y+C(Q)_{0-17}$	replaces EA
QL	0110	$y+C(Q)_{18-35}$	replaces EA
ICTC	0100	$y+C(ICTC)$	replaces EA
Du } see DL } note above	0011	$y, 00...0$	is the operand
	0111	$00...0, y$	is the operand

* y = address field of instruction word.

EA = an 18-bit intermediate operand address containing a segment address. EA is composed of: the address field of the instruction word; an internal base (if designated by bit 29 of the instruction word); any address modification employed prior to a final operand fetch.

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Spec. No. M50EB00107

Cont. on Sh. 2-67 Sh. No. 2-66

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

For IT type modification bits 32-35 are called the Tally Designator and specify tallying in detail

Table 2.6.1b Tally Designators for IT Modification

Tally Designator(t_d)		Name
Symbolic	bits 32-35	
I	1001	Indirect only
ITB	0001	Indirect to Base
ITS	0011	Indirect to Segment
DI	1100	Decrement Address, Increment Tally
AD	1011	Add Delta (to address field)
SD	0100	Subtract Delta (from address field)
ID	1110	Increment Address, Decrement Tally
DIC	1101	Decrement Address, Increment Tally, and Continue
IDC	1111	Increment Address, Decrement Tally, and Continue
CI	1000	Character from Indirect
SC	1010	Sequence Character
SCR	0101	Sequence Character Reversed
F1	0000	Fault 1
F2	0110	Fault 2
F3	0111	Fault 3

(only recognized when T_m , t_d indicate ITS, ITB)

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107 67

Cont. on Sh. 2-68 Sh. No. 2-67

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.6.1.1 Character Operations Specified by Address Modification

For 6-bit character operations in which the operand is taken from memory, the effective operand from memory is presented as a single word with the specified character justified to character position 5; positions 0-4 are presented as zero. For operations in which the resultant is placed in memory, character 5 of the resultant replaces the specified character in memory location Y; the remaining characters in memory location Y are not changed. Fig. 2.6.1.1 shows this relationship.

For 9-bit character operations in which the operand is taken from memory, the effective operand from memory is presented as a single word with the specified character justified to character position 3; positions 0-2 are presented as zero. For operations in which the resultant is placed in memory, character 3 of the resultant replaces the specified character in memory location Y; the remaining characters in memory location Y are not changed.

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Spec. No. M50EB00107

Cont. on Sh. 2-69 Sh. No. 2-68

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 GE-645 PROTOTYPE PROCESSOR

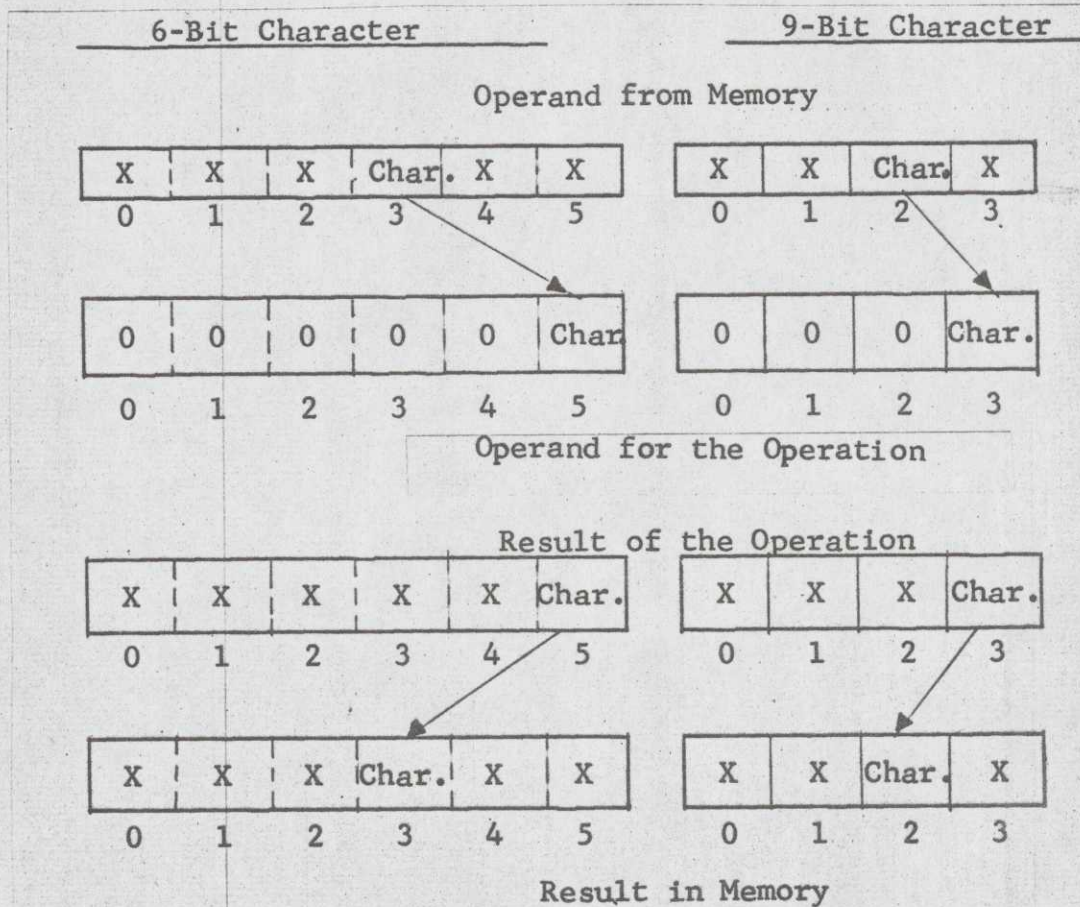


Fig. 2.6.1.1 CI, SC and SCR Modification Examples

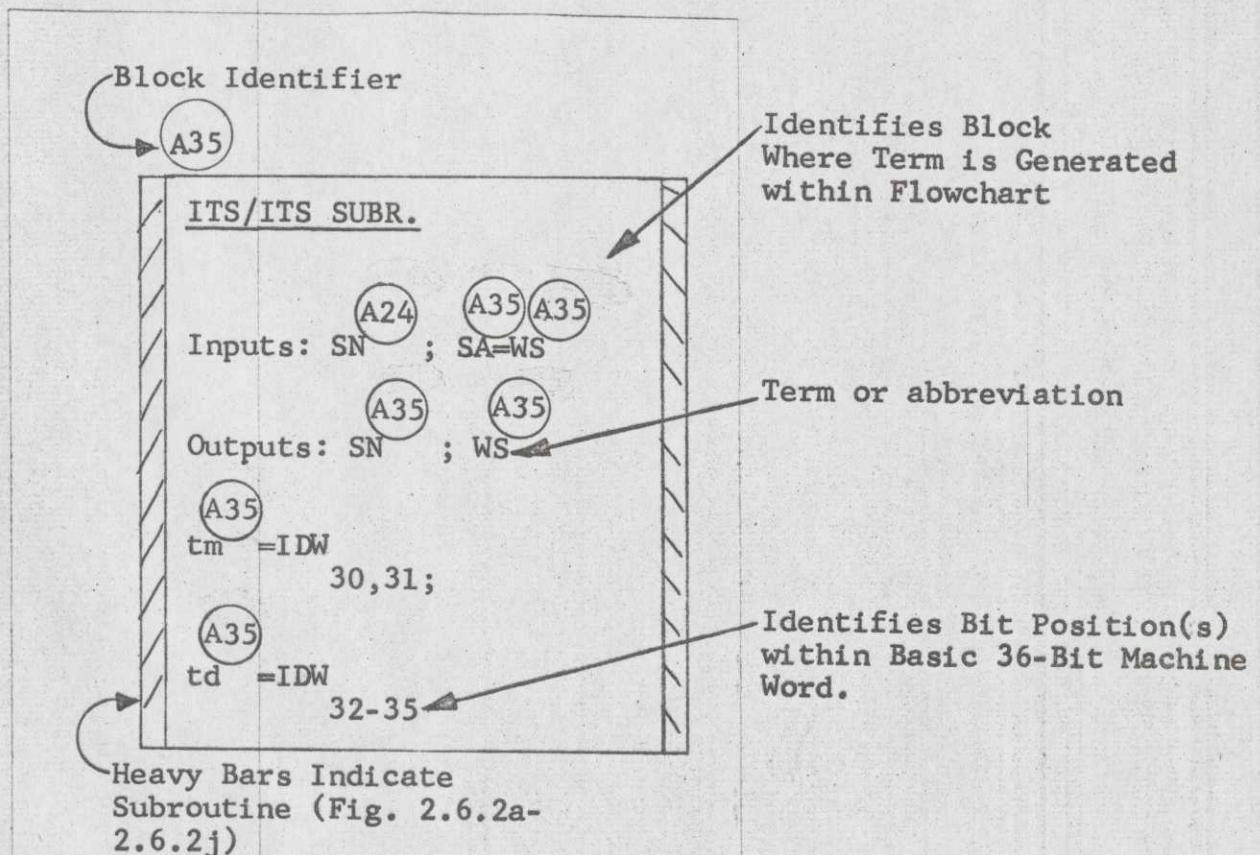
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GE-645 PROTOTYPE PROCESSOR

* 2.6.2 ADDRESS MODIFICATION FLOWCHARTS

Figure 2.6.2 is a flow chart of how address modification works in the GE-645. This flow chart is functionally orientated toward the software aspects of address modification rather than hardware. Additional flow charts are included for instruction fetches, address modification in detail, and cases where bit 29 of the instruction word is used. These flow charts, Fig. 2.6.2a - 2.6.2j are included immediately following Fig. 2.6.2 and are considered "subroutines" of the main flowcharts.

2.6.2.1 Flowchart Notation

The method of notation, and the representation of symbols on the flowcharts are as shown in the following example:



TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.6.2.1 - contd

Individual terms and abbreviations on the flow charts are defined as follows:

ABR	- Address Base Register
AD	- Add Delta (to Address Field) Modification
ADR	- Address Register
CF	- Character Field of Indirect then Tally word bits 33, 34, 35
CI	- Character from Indirect, Address Modification
DBR	- Descriptor Segment Base Register
DI	- Decrement Address, Increment Tally, Address Modification
DIC	- Decrement Address Increment Tally, and continue; Address Modification
DL	- Direct Lower, Address Modification
DSPTW	- Descriptor Segment Page Table Word
DU	- Direct Upper, Address Modification
EVEN	- Even instruction or indirect word
F1, F2, F3	- Fault, Address Modification
I	- Indirect only, Address Modification
ID	- Increment Address Decrement Tally, Address Modification
IDC	- Increment Address, Decrement Tally and continue; Address Modification
IDW	- Indirect Word
INST	- Instruction Word
IR	- Indirect then Register, Address Modification
IT	- Indirect then Tally, Address Modification
ITB	- Indirect to Base, Address Modification
ITS	- Indirect to Segment, Address Modification
ODD	- Odd instruction or indirect word
PBR	- Procedure Base Register
PTW	- Page Table Word
R	- Register, Address Modification
RI	- Register then Indirect, Address Modification
SA	- Segment Address
SC	- Sequence Character, Address Modification
SCR	- Sequence Character Reversed, Address Modification

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 2-72 Sh. No. 2-71

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.6.2.1 - contd

SD	- Subtract Delta (to address field), Address Modification
SDW	- Segment Descriptor Word
SN	- Segment Number
td	- Tag Field Designator
tm	- Tag Field Modifier
tb	- Character Size (0=6 bit, 1=9 bit)
WS	- 18-bit Working Sum (An intermediate quantity within the Flow Chart)

Spec. No. M50EB00107

Cont. on Sh. 2-73 Sh. No. 2-72

The flowchart illustrates the control logic of the GE-645 Prototype Processor. It begins with a START node leading to a block that sets initial values for t_d (INST 0-35) and t_m (INST 30-31). A decision diamond checks if $t_m = 1$. If yes, it branches to a block setting $R=00$ and $IT=10$. If no, it branches to a block setting $R=01$ and $IR=11$. The main flow proceeds through several subroutines: **BIT 29 SUBR.** (for t_d and t_m), **ITS/ITB SUBR.** (for t_m and t_d), and **DI SUBR.** (for t_m and t_d). The flowchart includes decision points for $t_d = ?$, $t_m = ?$, and $t_d = F_1, F_2, \text{ or } F_3$. It also includes a block for **CAUSE FAULT TAG FAULT TRAP** with a table of fault codes: F_1 01000, F_2 01110, F_3 01111. The flowchart concludes with an **END** node.

NOTE: $t_d = DU$ OR DL SHOULD NOT BE USED WITH $t_m = RI$ OR IR

NOTE: $t_d = ITS$ or ITB SHOULD NOT BE USED HERE.

Fig. 2.6.2 GE-645 ADDRESS MODIFICATION FLOW CHART (SHEET 1 of 2)

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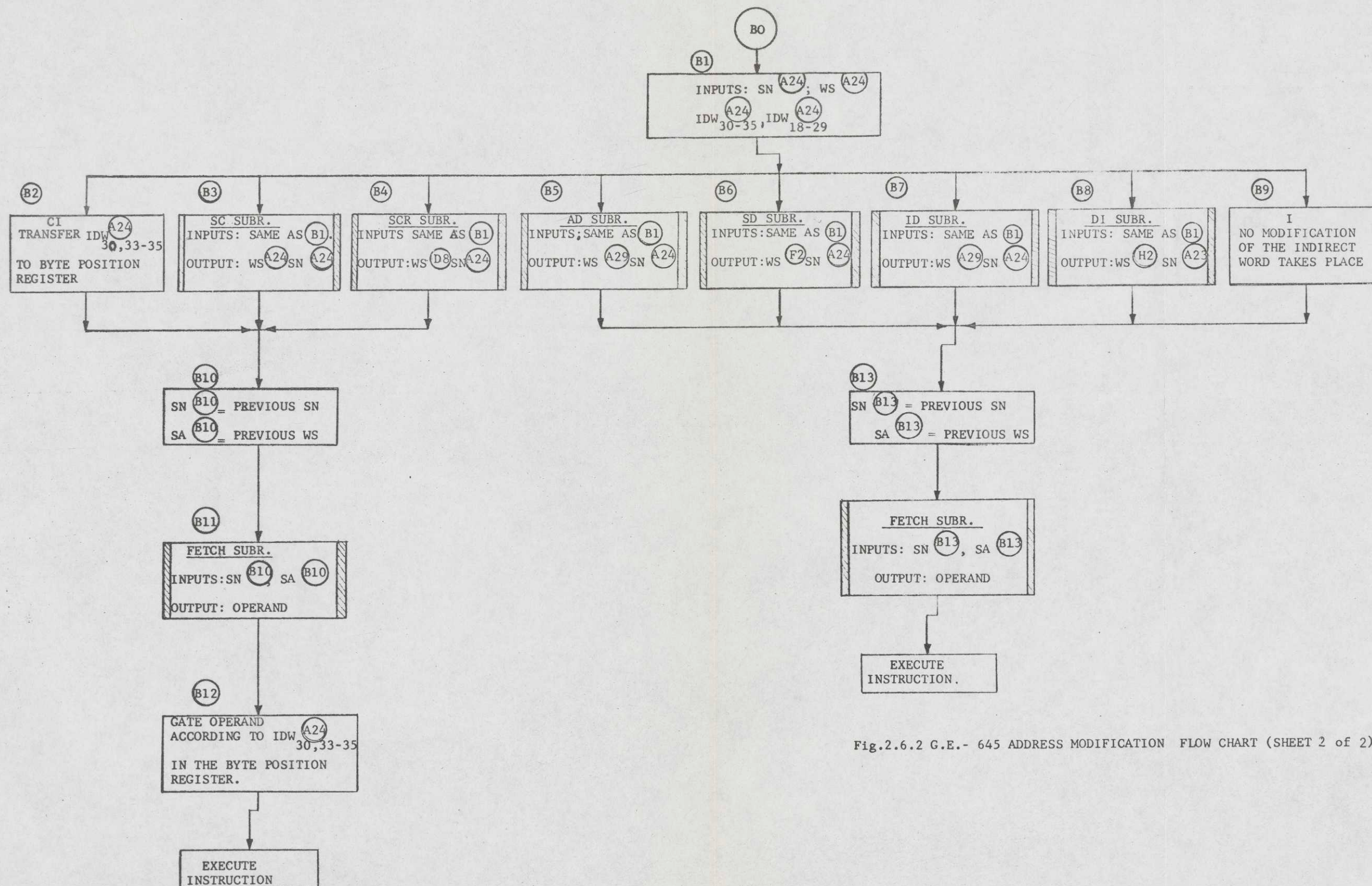


Fig.2.6.2 G.E.- 645 ADDRESS MODIFICATION FLOW CHART (SHEET 2 of 2)

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Spec. No. M50EB00107

Cont. on Sh. 2-75 Sh. No. 2-74

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GE-645 PROTOTYPE PROCESSOR

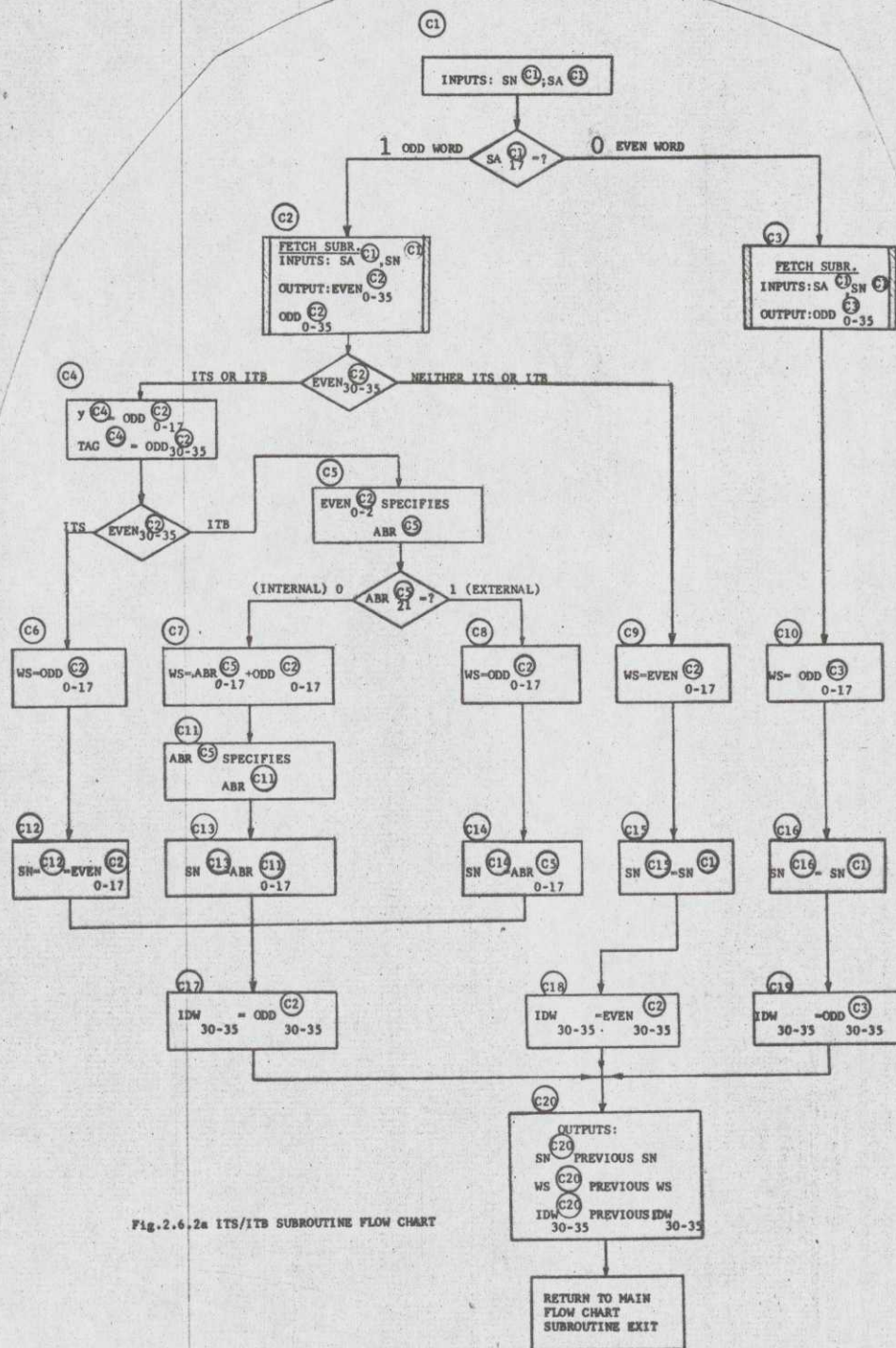


Fig. 2.6.2a ITS/ITB SUBROUTINE FLOW CHART

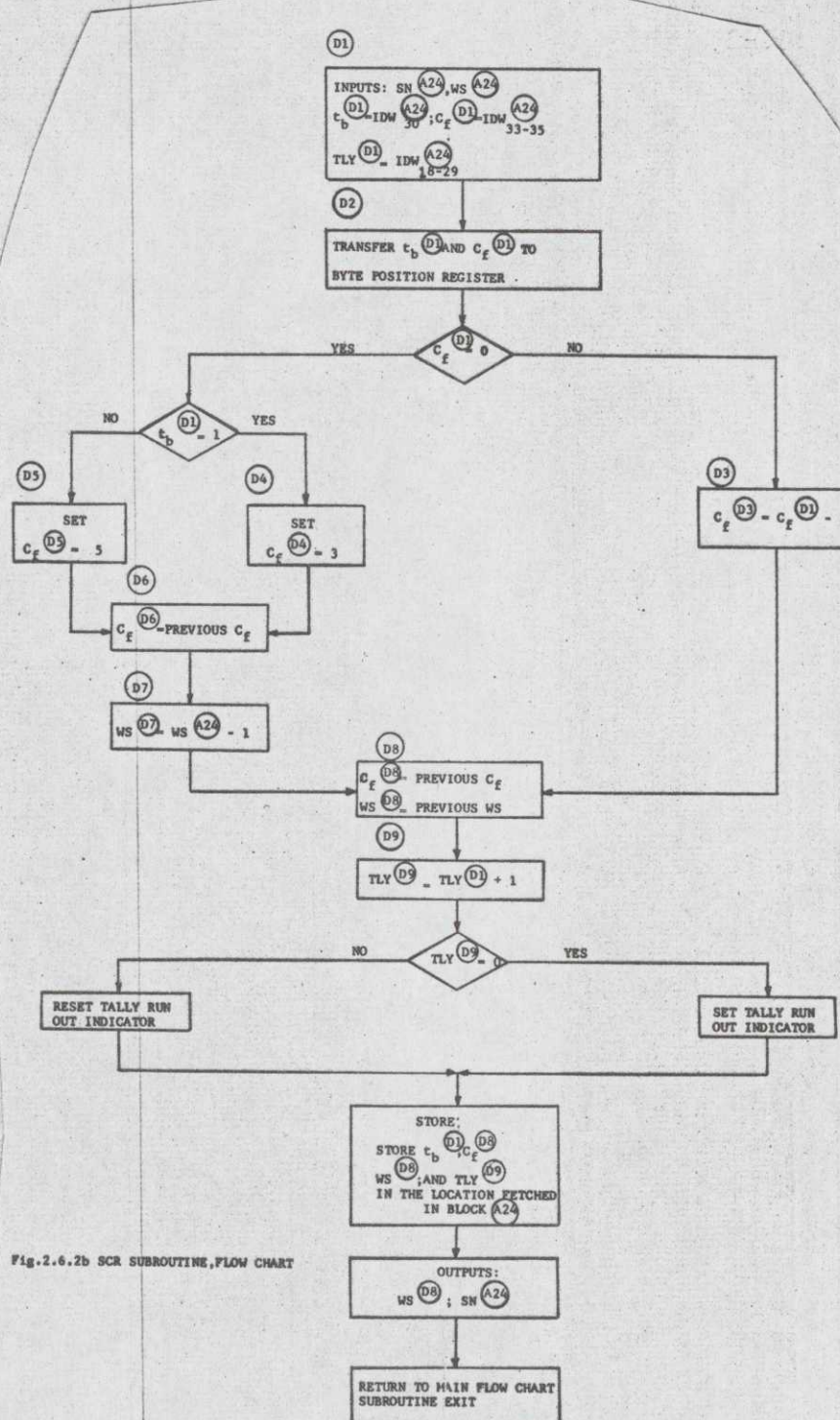
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Spec. No. M50EB00107

Cont. on Sh. 2-76 Sh. No. 2-75

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GE-645 PROTOTYPE PROCESSOR



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Spec. No. M50EB00107

Cont. on Sh. 2-77

Sh. No. 2-76

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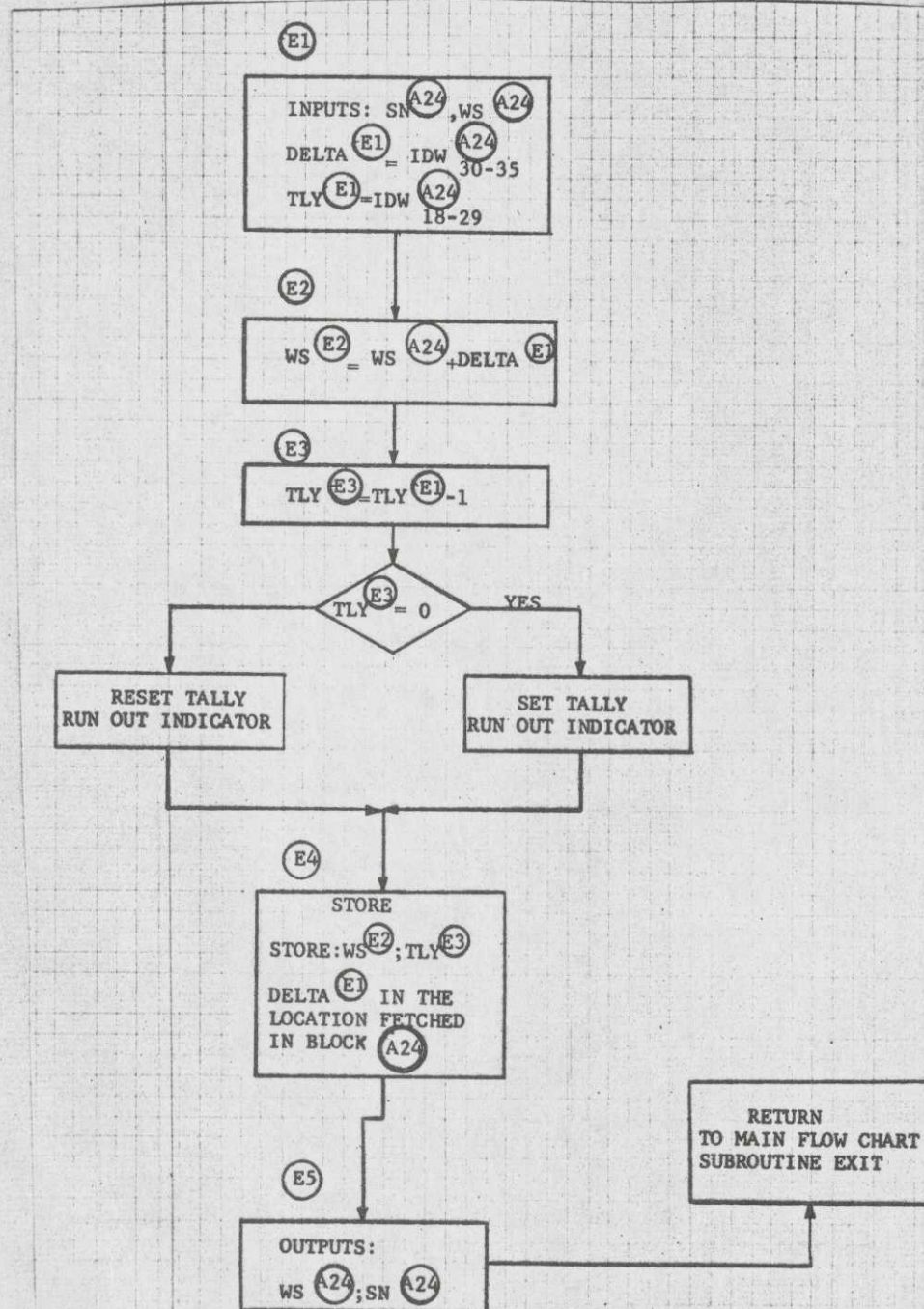


Fig. 2.6.2c AD SUBROUTINE, FLOW CHART

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Cont. on Sh. 2-78

Sh. No. 2-77

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GE-645 PROTOTYPE PROCESSOR

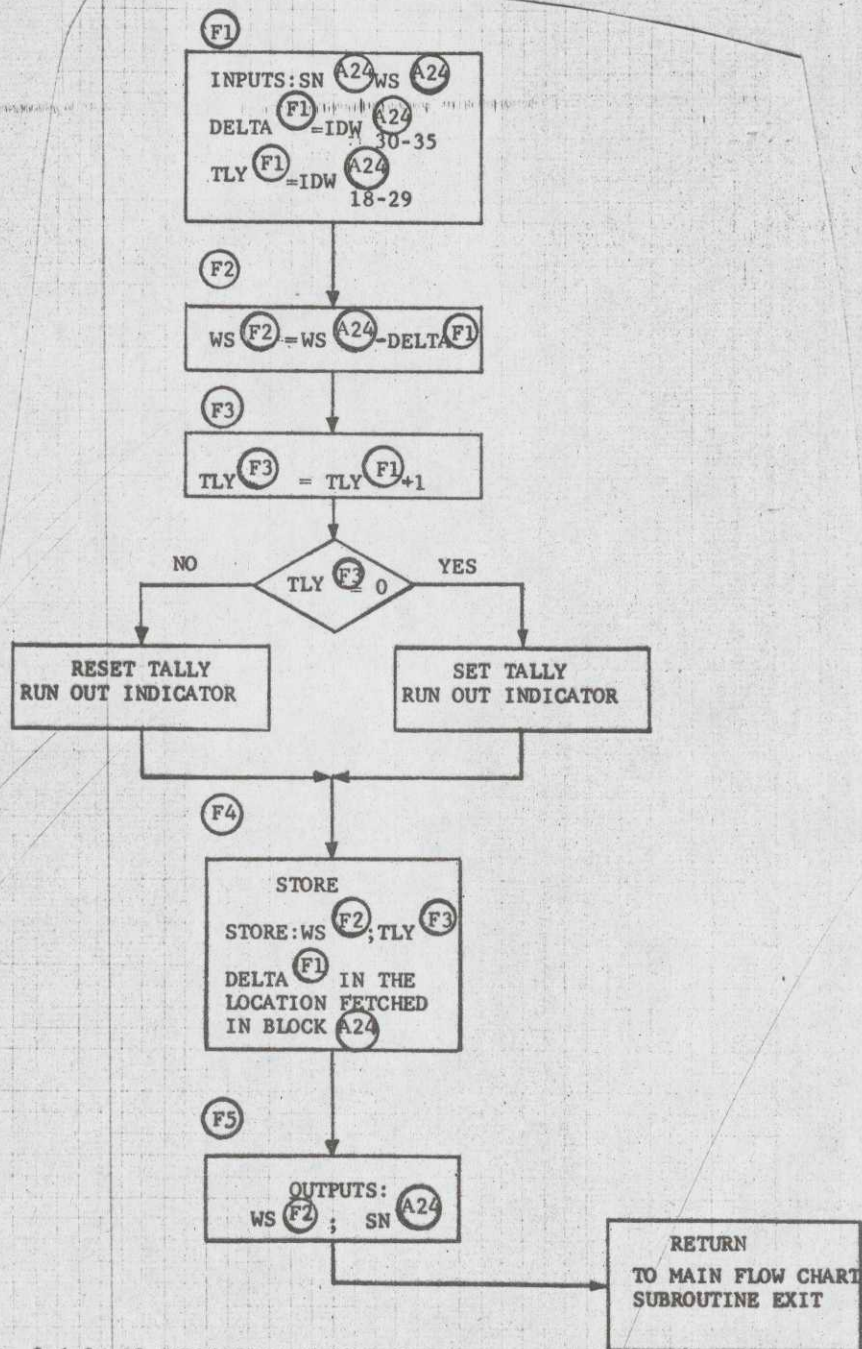


Fig. 2.6.2d SO SUBROUTINE, FLOW CHART.

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Spec. No. M50EB00107

Cont. on Sh. 2-79 Sh. No. 2-78

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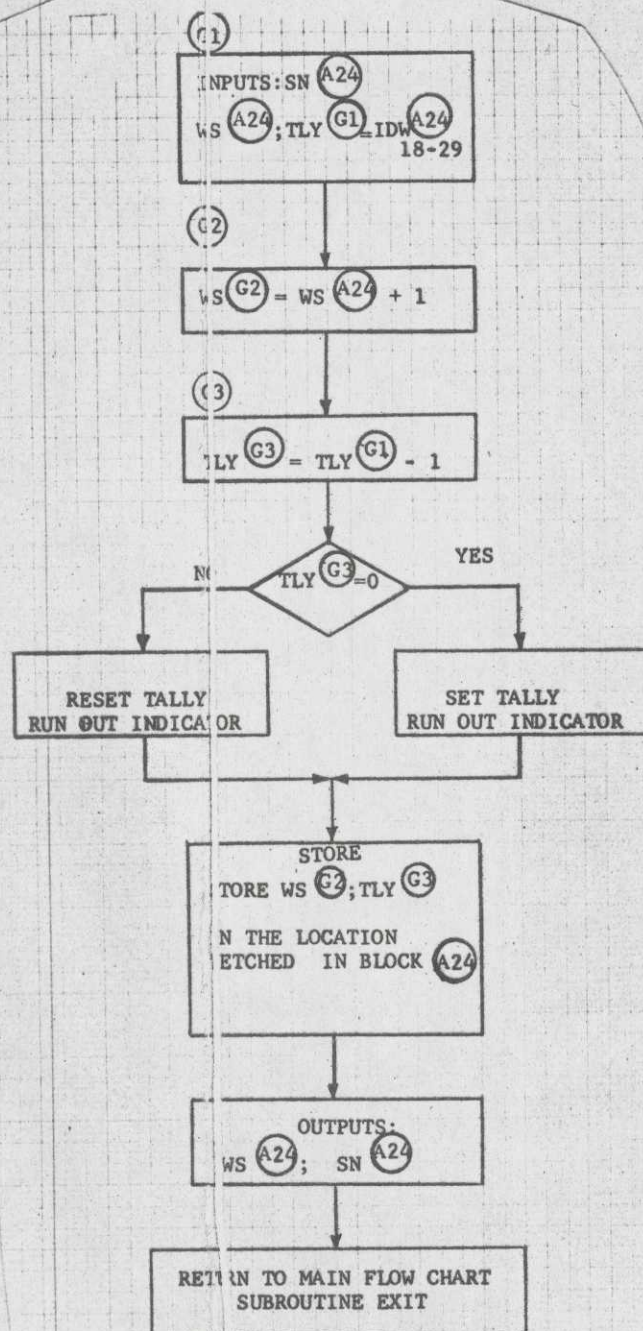


Fig. 2.6.2e ID SUBROUTINE FLOW CHART

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Cont. on Sh. 2-80 Sh. No. 2-79

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GE-645 PROTOTYPE PROCESSOR

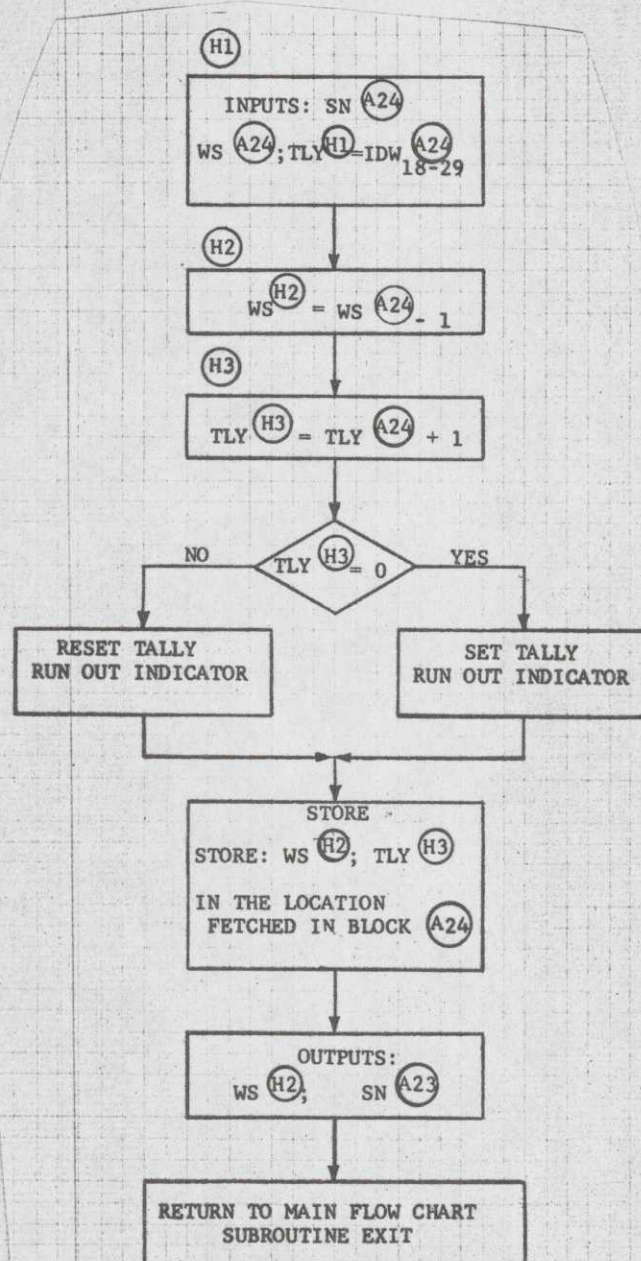


Fig.2.6.2f DI SUBROUTINE, FLOW CHART

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Spec. No. M50EB00107

Cont. on Sh. 2-81

Sh. No. 2-80

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GE-645 PROTOTYPE PROCESSOR

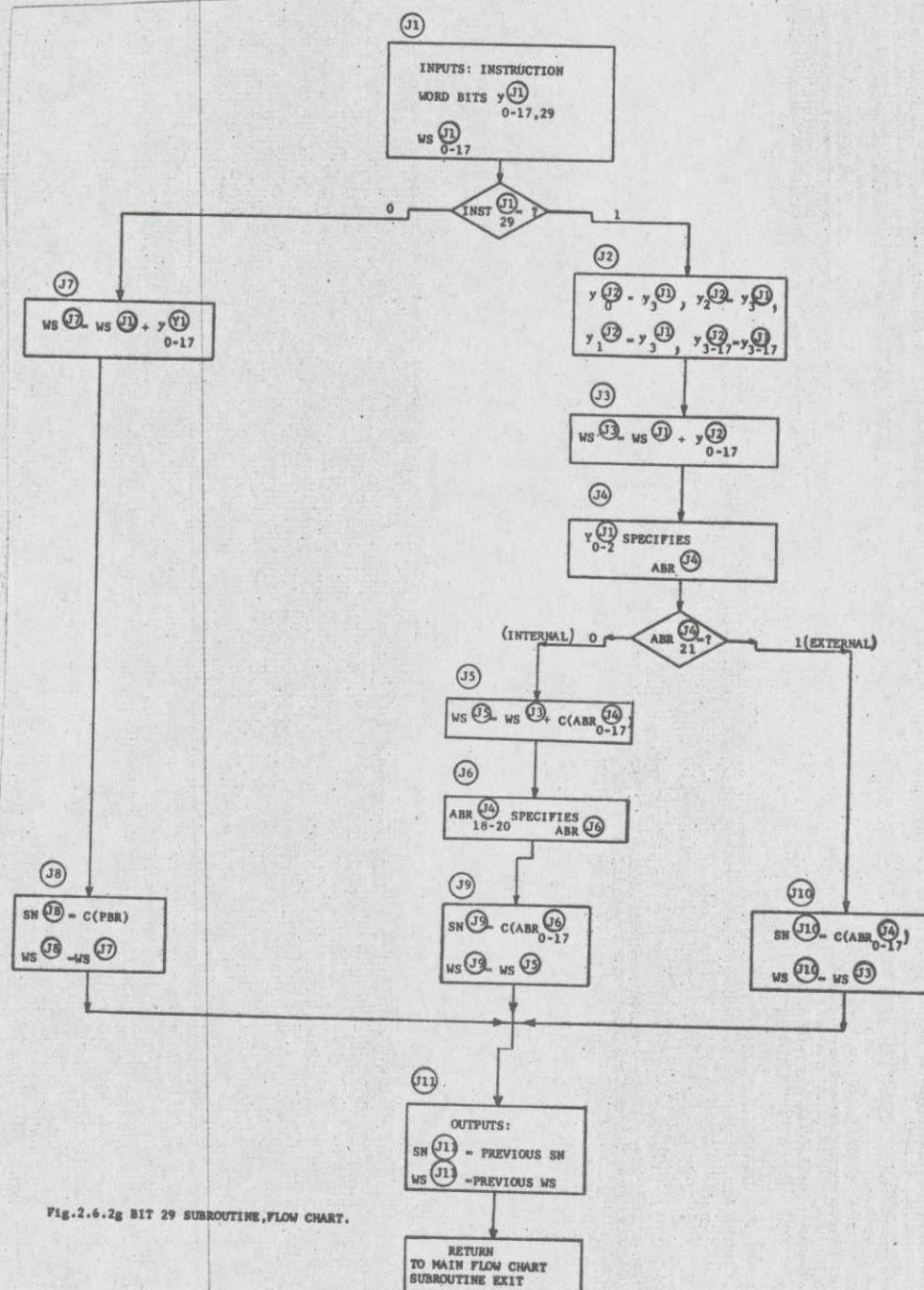


Fig. 2.6.2g BIT 29 SUBROUTINE, FLOW CHART.

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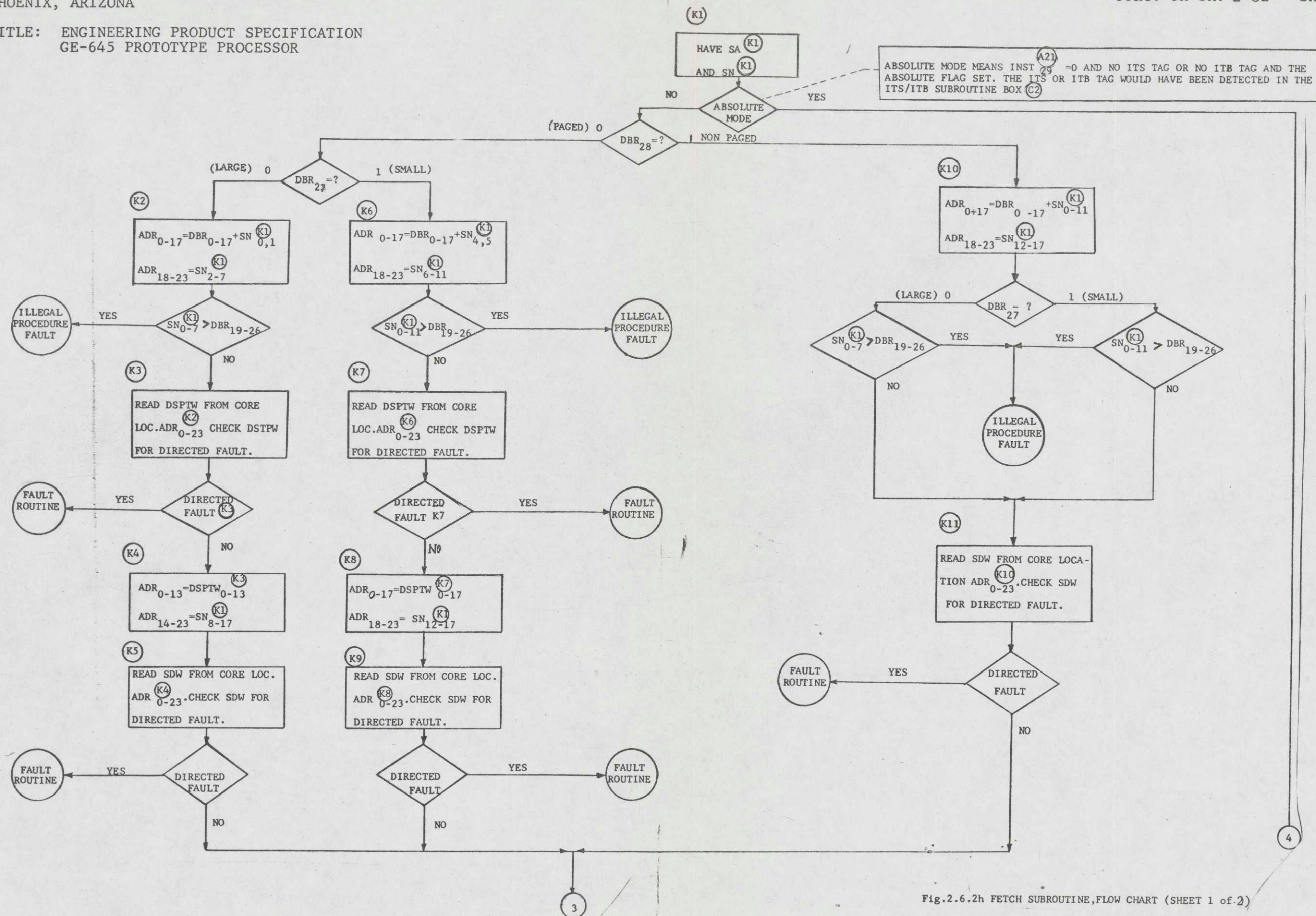


Fig.2.6.2h FETCH SUBROUTINE, FLOW CHART (SHEET 1 of 2)

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GE-645 PROTOTYPE PROCESSOR

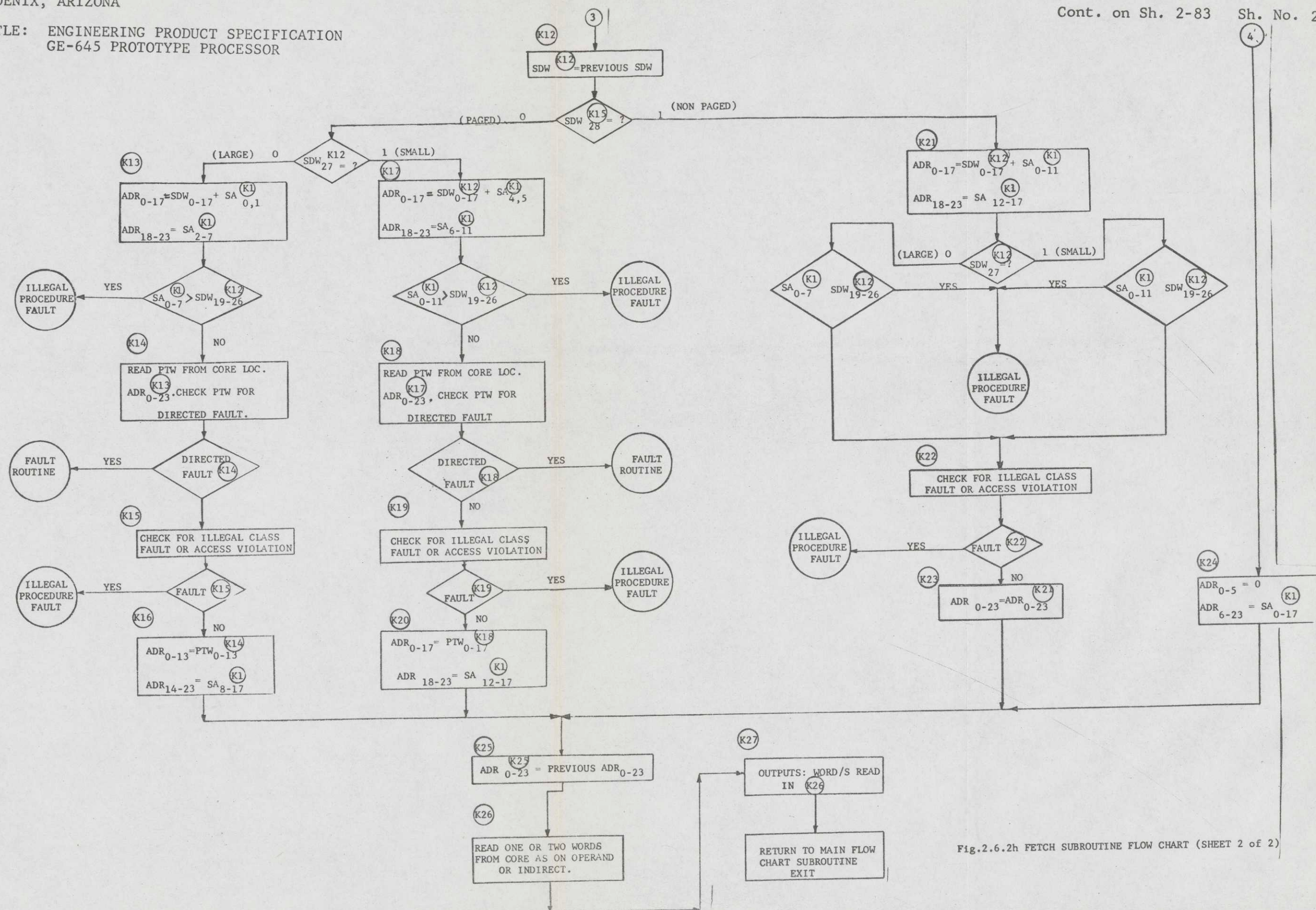


Fig. 2.6.2h FETCH SUBROUTINE FLOW CHART (SHEET 2 of 2)

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Spec. No. M50EB00107

Cont. on Sh. 2-84 Sh. No. 2-83

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GE-645 PROTOTYPE PROCESSOR

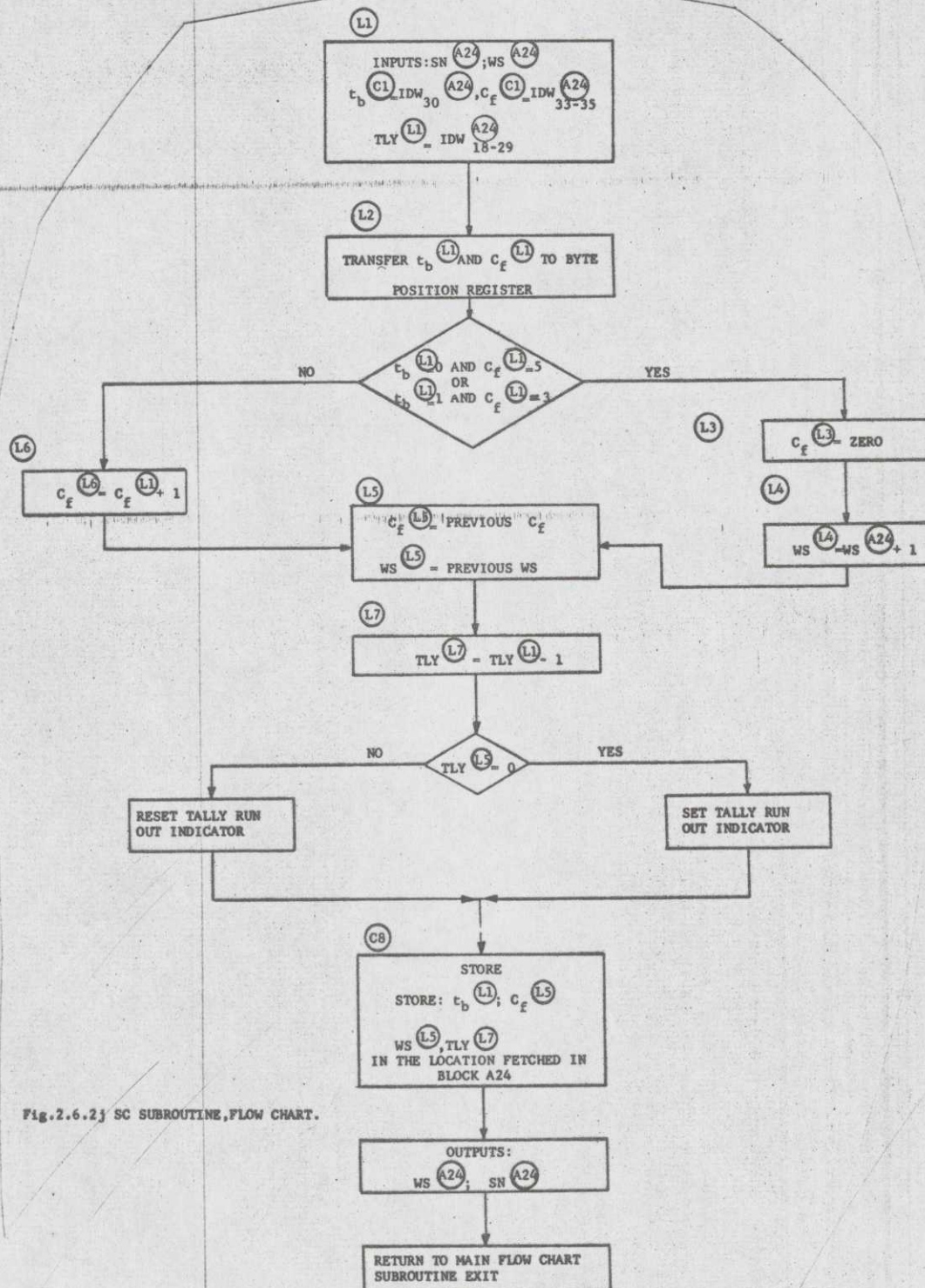


Fig. 2.6.2; SC SUBROUTINE, FLOW CHART.

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GE-645 PROTOTYPE PROCESSOR

2.7 ADDRESS APPENDING

2.7.1 GENERAL

Address appending is that function of the Processor that allows the addressing of segments and pages (see 2.2). The appending process takes a relative address from a program and the segment number of the segment to which that address refers and forms the absolute address. Appending is required for an address if:

- 1) The Processor is not addressing in Absolute mode.
- 2) It is for an operand or indirect word of an instruction that has its bit 29 = "1."
- 3) An ITS or ITB modification is in process.

This process requires the use of various registers and control words. For a definition of these registers see 2.4 of this specification. For a definition of the control words see 2.5.5 of this specification.

Figure 2.7.1 sheets 1-5 contain a hardware orientated flow chart of the appending process.

Figure 2.7.1a shows the placement of the various addresses and parts of addresses with respect to the final 24-bit address.

For a discussion of the Processor segmentation and paging requirements see ESS M50EB00105 Section 3.5.8. This discussion assumes a familiarity with these requirements.

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Spec. No. M50EB00107

Cont. on Sh. 2-86 Sh. No. 2-85

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.7.1 - contd

NOTES APPLICABLE TO SHEETS 2-5

- 1) A Program Interrupt may break in and stop the Appending Process up until point A.
- 2) Large Page. (1024 Words)
- 3) Small Page. (64 Words)
- 4) $ESTR_{0-3}$ and $OSTR_{0-3}$ are loaded at the same time as Y_{0-35} and C_{0-35} . $ESTR_{0-2}$ will hold the same information as Y_{0-2} , $ESTR_3$ will reflect Y_{29} , $OSTR_{0-2}$ will hold the same information as C_{0-2} , and $OSTR_3$ will reflect C_{29} .
- 5) $ESTR$ and $OSTR$ can also be loaded by an ITB Modifier.
- 6) "Address" refers to the Address formed by the Control Unit as it appears at the output of the BS-Adder.
- 7) Pointer refers to the identification of a SDW or PTW as it appears on the ZBRX Bus. (External base bus)
- 7) AR_n refers to the selected Associative Register in the Associative Memory.
- 8)  Shading indicates entry points.

Fig. 2.7.1 Address Appending Flow Chart

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Spec. No. M50EB00107

Cont. on Sh. 2-87 Sh. No. 2-86

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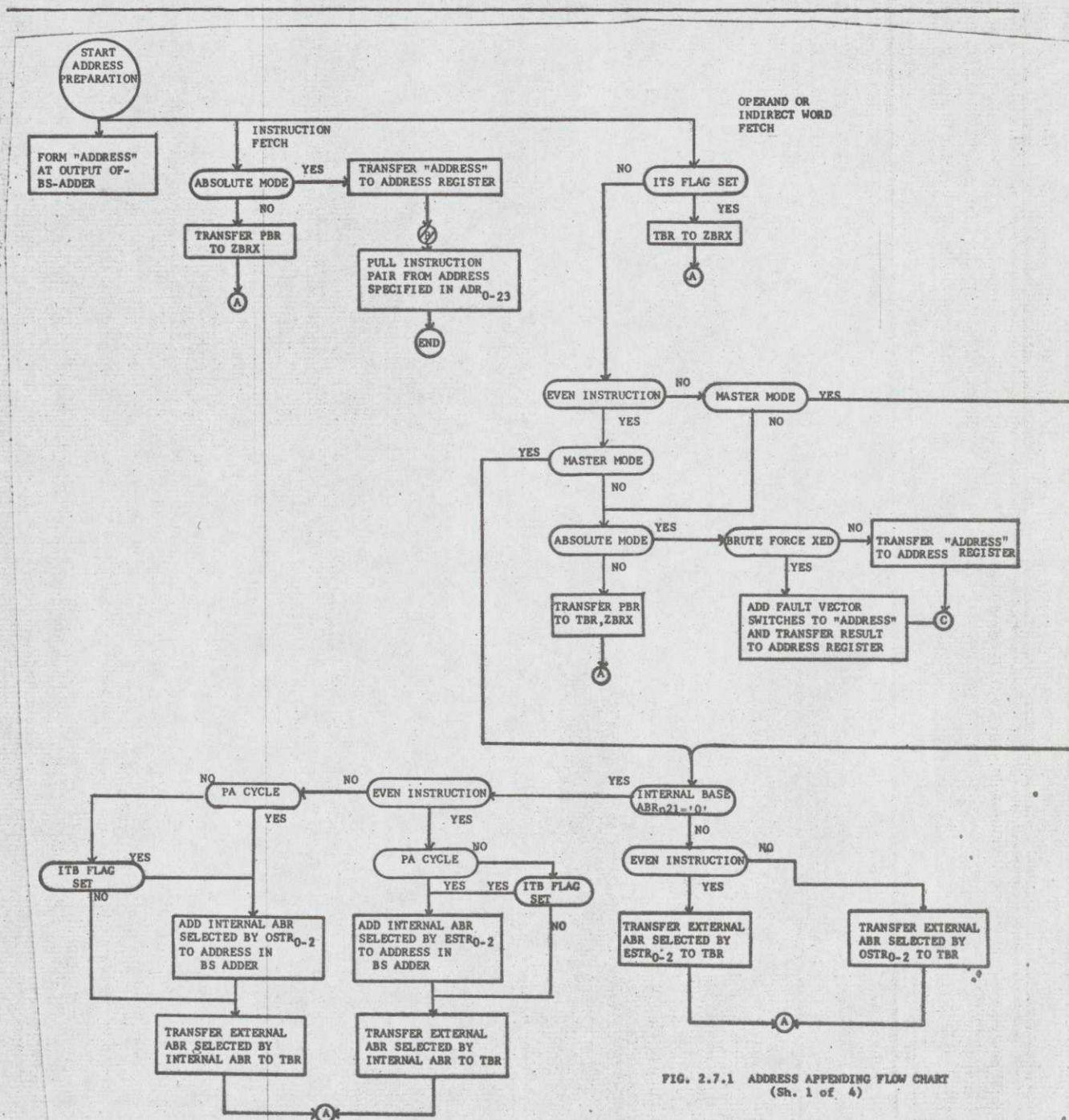


FIG. 2.7.1 ADDRESS APPENDING FLOW CHART
(Sh. 1 of 4)

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Cont. on Sh. 2-88 Sh. No. 2-87

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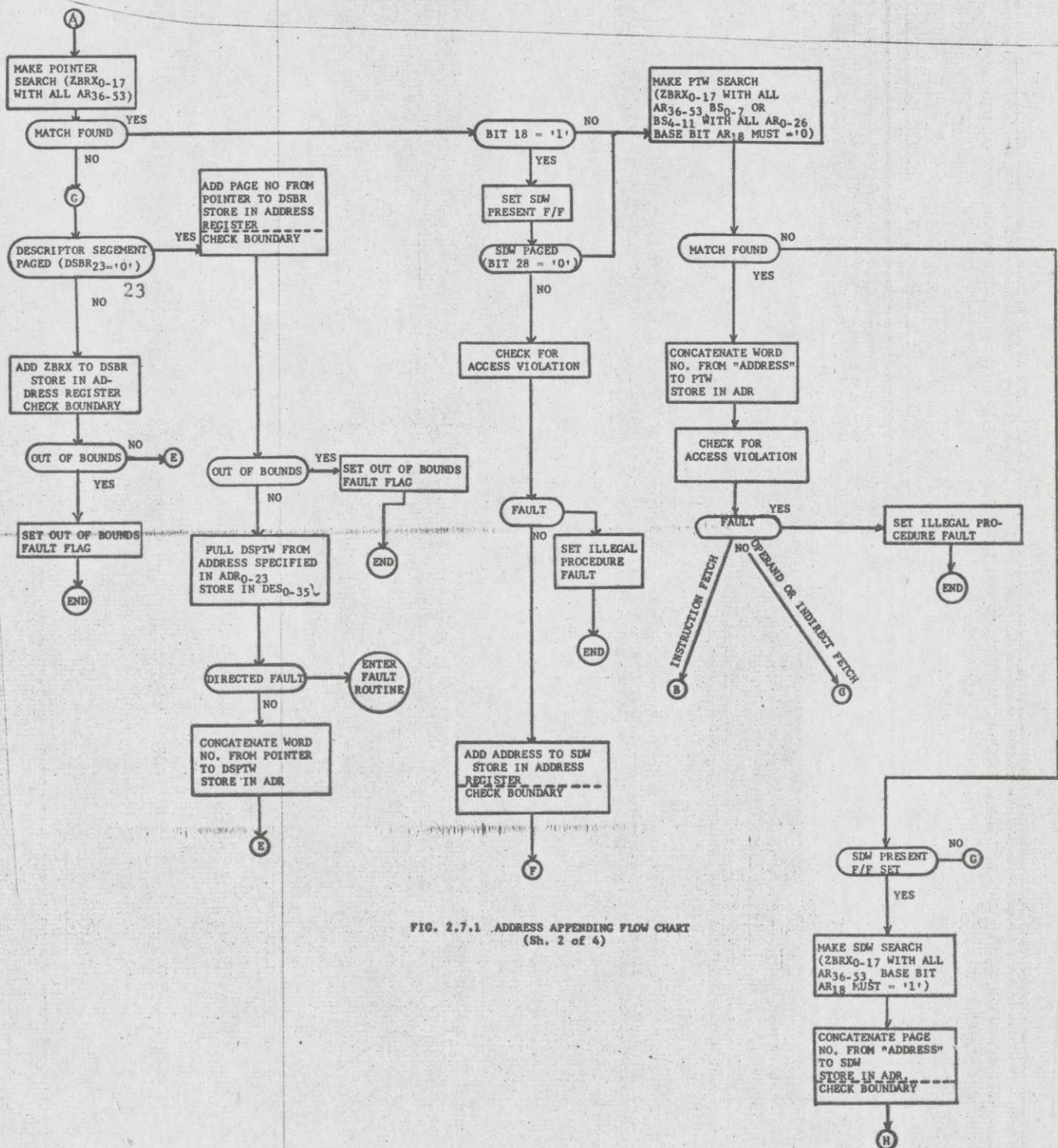


FIG. 2.7.1 ADDRESS APPENDING FLOW CHART
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Spec. No. M50EB00107

Cont. on Sh. 2-89 Sh. No. 2-88

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GE-645 PROTOTYPE PROCESSOR

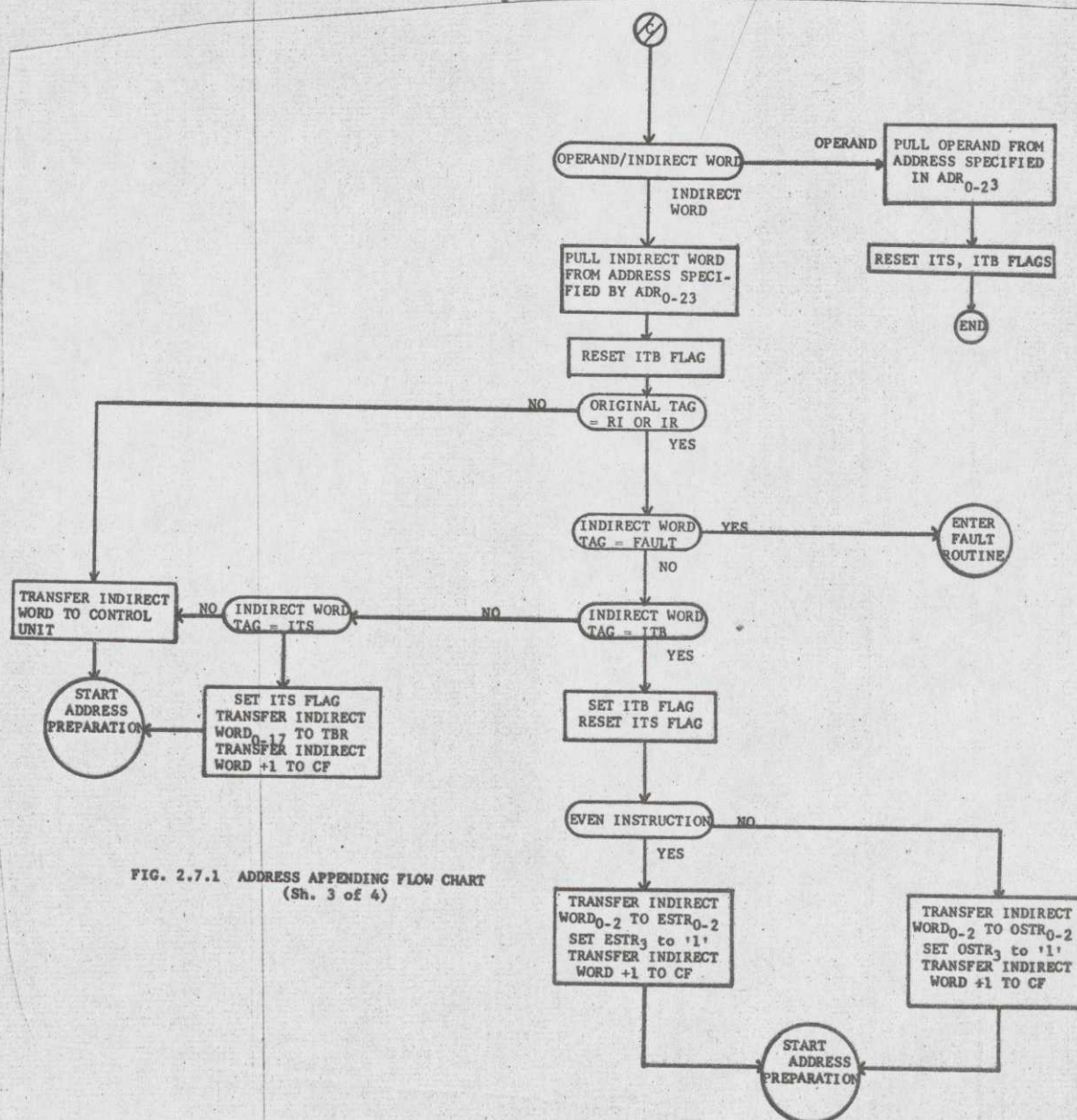


FIG. 2.7.1 ADDRESS APPENDING FLOW CHART
(Sh. 3 of 4)

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Spec. No. M50EB00107

Cont. on Sh. 2-90 Sh. No. 2-89

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GE-645 PROTOTYPE PROCESSOR

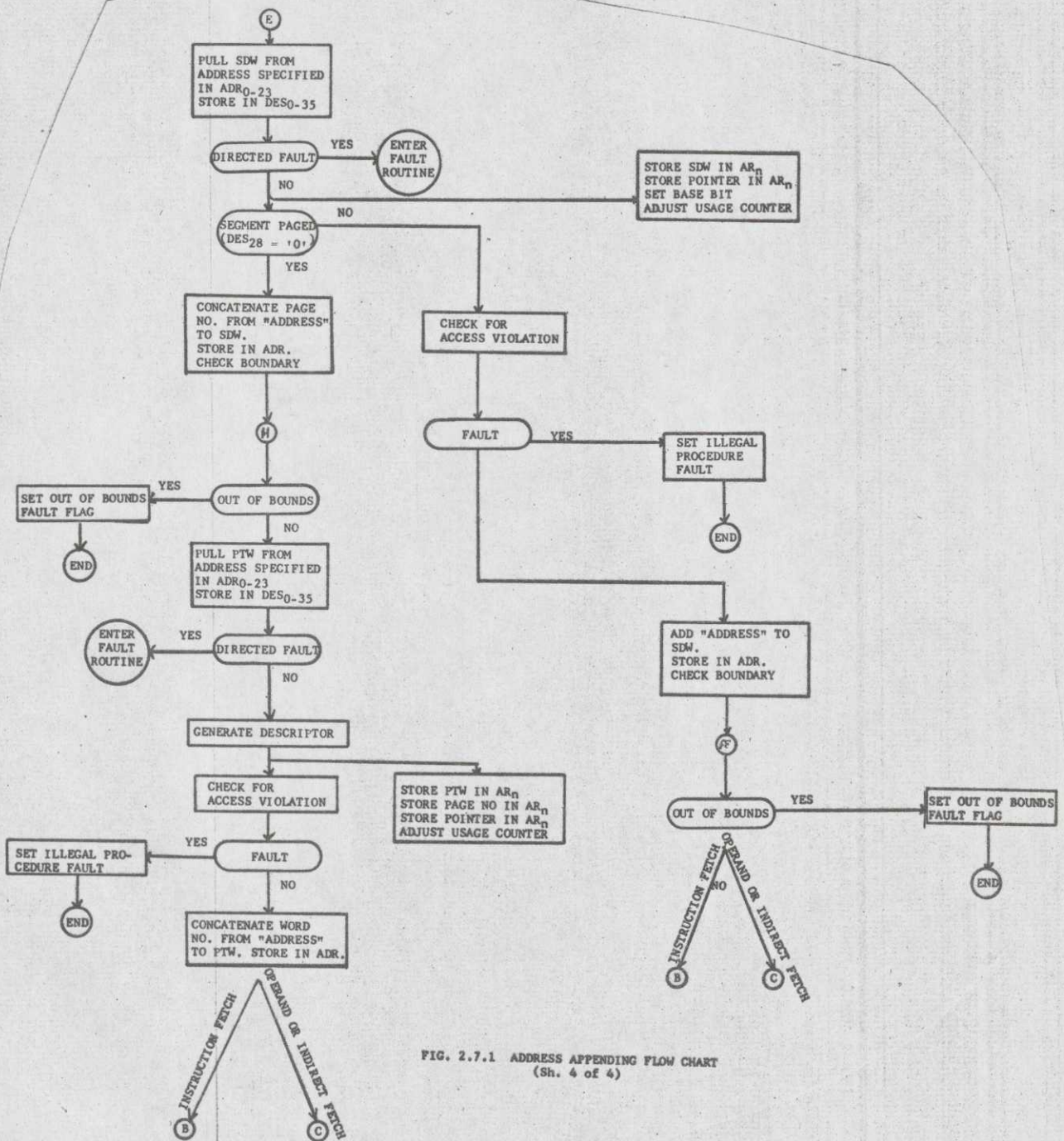


FIG. 2.7.1 ADDRESS APPENDING FLOW CHART
(Sh. 4 of 4)

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 GE-645 PROTOTYPE PROCESSOR

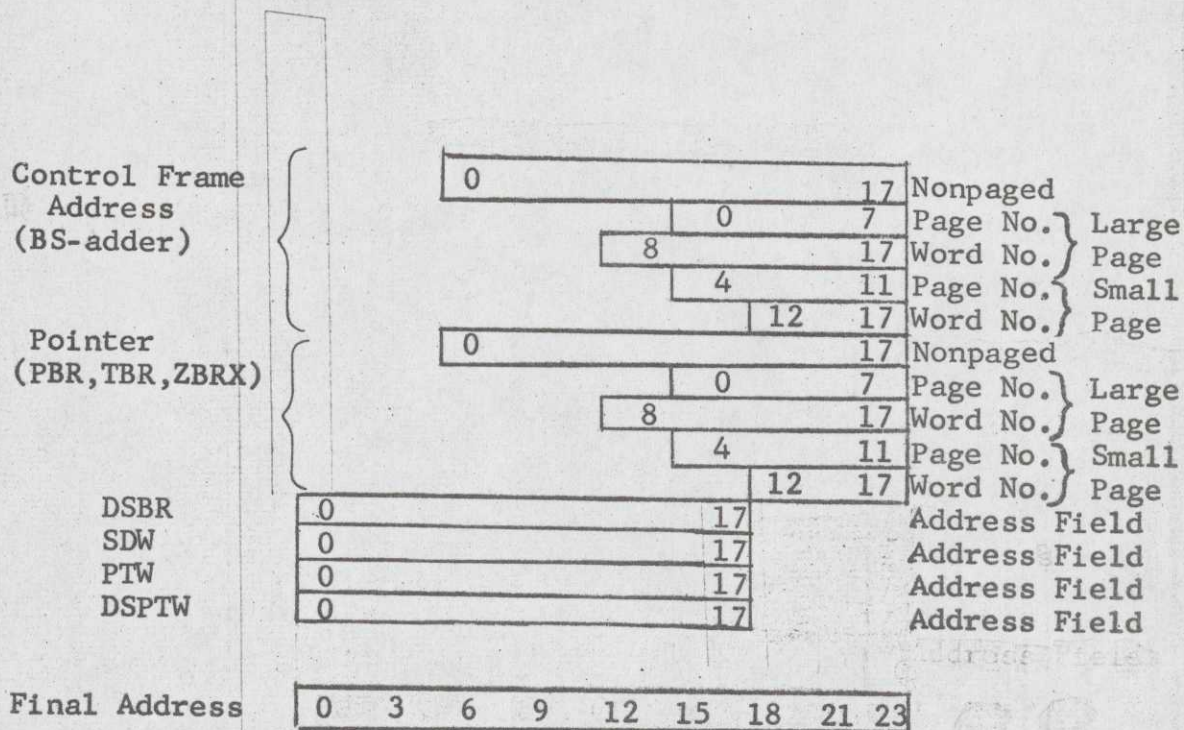


Fig. 2.7.1a Parts of the Address versus the 24-bit Core Address.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.7.2 APPENDING CYCLE I (NONPAGED SEGMENT, NONPAGED DESCRIPTOR SEGMENT).

This cycle can be used to obtain an operand, indirect word, or instruction. The Control Unit will produce an address consisting of a page number and word number at the output of the BS-adder, though this page and word number defines contiguous mod 64/1024 blocks in the nonpaged segment. It is understood that the DSBR and PBR contain the following information:

- DSBR₀₋₁₇ - Base address mod 64 of the descriptor segment.
- DSBR₁₈₋₂₆ - Size of the descriptor segment.
- DSBR₂₇ - Size of the descriptor segment page or block
0 = mod 1024, 1 = mod 64.
- DSBR₂₈ - Paged; 0 = paged, 1 = not paged.
- ZBRX₀₋₁₇ - The relative address of the SDW (page and word number) within the descriptor segment. It is called the pointer, and identifies the SDW for that segment.
- (Pointer)

The Associative Memory will be searched to see if it contains the required SDW. This is done by comparing the PBR against the pointer field of each of the 16 AM-registers. If a valid match is found the SDW in the Associative Memory will be used. If a valid match is not found the SDW must be obtained from core memory. Assume the latter to be the case. The DSBR is checked to see if the descriptor segment is paged. In this case bit 28 will be a "1" indicating that it is not paged. Therefore, the address field of the DSBR, left-justified, is added to the Pointer, right-justified, to form a 24-bit address (see fig. 2.7.1a). This is the absolute address of the SDW in core memory. At the same time the Pointer is compared against the size field of the DSBR. If the Pointer is larger than the size an out of bounds fault will occur. If it is not larger, the SDW will be obtained from the resultant address.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.7.2 - contd

Upon receipt of the SDW, its descriptor field is checked to see if there is a Directed fault. If there is, the fault routine will be entered, if not bit 28 is checked to see if the segment is paged. In this case bit 28 will be a "1" indicating not paged. At this time the descriptor will be checked to determine the type of segment being dealt with to determine if the operation to be performed is legal. If the operation is legal, the address field of the SDW, left-justified, is added to the address from the Control Unit BS-adder output (right-justified), to form a 24-bit address. The BS-adder output consists of the sum of the address field of the instruction or indirect word, any address modification, any internal base designated by the instruction word, or an ITB modifier. This is the absolute address of the desired operand, indirect word, or instruction word. At the same time the address in the BS-adder is compared against the size field of the SDW. If it is larger an Out Of Bounds fault occurs. If it is not larger the desired word will be fetched.

At the same time the SDW with its identifying pointer (the contents of the PBR) is stored in an Associative Memory Register (AR), where it can be used for any other references to that segment.

If the SDW was found in the Associative Memory a check will be made to see if it is paged. In this case bit 28 will be a "1" indicating that it is not paged. The descriptor field will not be checked for a Directed fault, but it will be checked for Access Violation. From this point on the final address is formed in the same manner as for the SDW from core memory.

2.7.3 APPENDING CYCLE II (NONPAGED DESCRIPTOR SEGMENT, PAGED SEGMENT).

The same conditions prevail as in the first paragraph of 2.7.2.

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Spec. No. M50EB00107

Cont. on Sh. 2-94 Sh. No. 2-93

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.7.3 - contd

The Associative Memory will be searched to see if it contains the required PTW. This is done by comparing the PBR against the pointer field of each of the 16 ARs. It is possible for the Associative Memory to contain the SDW and more than one PTW with the same pointer. If this is the case all such ARs will produce a valid match. The Associative Memory checks to see if any of the registers having a valid match contains a SDW (bit 18 = "1"), If a SDW is found that fact is remembered and a search is made for the specific PTW required. This is done by doing another compare cycle. This time the PBR is compared against the pointer field, the page number of the BS-adder address is compared against the page number field of each AR, and bit 18 is checked to see that it is "0". If all the conditions are met it indicates that the required PTW is available, and it will be used to prepare the final address.

If the PTW search fails the Associative Memory checks to see if it had originally found the SDW. If it had it refinds it, and it will be used in the formation of the address for the PTW. If it had not found it the Processor must obtain it from the core memory. This will be accomplished in the same manner as in the previous case, and it will be stored in the Associative Memory.

It should be noted here that if the SDW is obtained from core memory the descriptor field will be checked for a Directed fault, but if it is obtained from the Associative Memory no check will be made. In neither case will the descriptor be checked for Access Violation.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.7.3 - contd

The SDW, whether it was obtained from the Associative Memory or from core memory, is used in the formation of the address of the PTW. The page number in the BS-adder address is concatenated to the address field of the SDW. The 18-bit address field of the SDW is left-justified, and the 8-bit page number of the BS-adder address is right-justified to form the 24-bit address. This provides an overlap of two bits, which are added. The resultant address is the absolute address of the PTW. At the same time the page number is compared against the size field of the SDW. If it is larger than the size an Out Of Bounds fault will occur, otherwise the PTW will be obtained from the resultant address.

If the PTW is received from core memory its descriptor field is checked for a Directed Fault. If there is one, the fault routine is entered. If not a descriptor generation cycle is entered. During this cycle the descriptor from the SDW is compared with the descriptor of the PTW. The most restrictive of the two is retained. The PTW and the most restrictive descriptor is written into the Associative Memory. Its pointer field will contain the contents of the PBR and its page number field will contain the page number from the BS-adder. The "used" bit (25) will be made a "1" indicating that the page has been accessed, and if the current access will alter the contents of the page its "written" bit (26) will be made a "1". If either bit 25 or 26 was a "0" and is changed to a "1", the corresponding bit in core memory must also be changed. The new descriptor is checked to see if the operation to be performed is legal. If it is not, an Access Violation fault will occur. If it is, then the final address will be prepared.

If the PTW is received from the Associative Memory it is assumed that Out Of Bounds checks and Directed fault checks were made and passed when the PTW was first obtained and stored in the Associative Memory.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.7.3 - contd

Therefore, they are not necessary now, and are bypassed. The descriptor field will be checked for Access Violation.

Assuming that all is well at this point, the final address will be formed by concatenating the word number from the BS-Adder to the PTW. The 18-bit PTW address is left-justified, and the 6- or 10- bit word number (6-bit if a small page, 10-bit if a large page) is right-justified to form the 24-bit final address. This is the absolute address of the desired operand, indirect word, or instruction.

2.7.4 APPENDING CYCLE III (PAGED DESCRIPTOR SEGMENT, PAGED/
NONPAGED SEGMENT)

It is assumed that the DSBR and PBR have the proper information in them.

The Associative Memory will be searched to see if it contains a valid SDW or PTW. If it does the address formation will proceed in the same manner as described in 2.7.3. If nothing is found it must all be retrieved from core memory.

The DSBR is checked to see if the descriptor segment is paged. In this case bit 28 will be "0" indicating that it is paged. Therefore the DSPTW must be pulled from core memory. DSPTWs are never stored in the Associative Memory. The 18-bit address field of the DSBR, left-justified, is added to the page number field of the PBR, right-justified, to form a 24-bit address. This is the absolute address of the DSPTW. At the same time the page number field of the PBR is compared against the boundary field of the DSBR. If it is larger an Out Of Bounds fault occurs, otherwise the DSPTW is fetched from core memory.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.7.4 - contd

Upon receipt of the DSPTW its descriptor field is checked for a Directed fault. If there is one, the fault routine will be entered, otherwise the address for the SDW will be formed. This is done by concatenating the word number field of the PBR to the DSPTW. The 18-bit DSPTW is left-justified and the 10/6-bit word number is right-justified. This forms the 24-bit address of the SDW. From this point on it is the same as 2.7.2 or 2.7.3 where no match was found in the Associative Memory.

2.7.5 APPENDING CYCLE IV (OBTAIN DATA FROM A DIFFERENT SEGMENT)

This cycle can only be done for operands or indirect words and can be done whether or not the Control Unit is in Absolute. This cycle is started upon the execution of an instruction which has bit 29 = "1". When this happens the three most-significant bits of the address field are decoded to select one of the eight Address Base Registers (ABRn). The selected ABRn may be either an external base (bit 21 = "1") or an internal base (bit 21 = "0").

If the selected ABRn is an external base its contents are transferred to the TBR and are used as the pointer instead of the PBR. The PBR is not altered and the next instruction will revert to using PBR if the instruction does not have bit 29 = "1". (Exception: transfer instructions, see 2.7.6). All memory accesses for this instruction will be referenced to this ABRn (Exception: ITS or ITB, see 2.7.7). This allows an instruction in one segment to reference an operand in a different segment. All search and fetch cycles are the same as for 2.7.2 - 2.7.4, except that the ABRn is used as the pointer instead of the PBR.

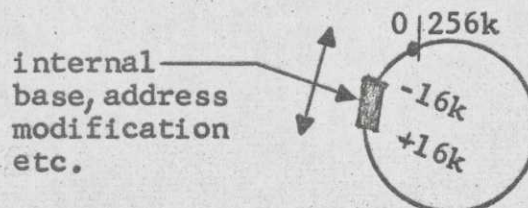
A brief description of addressing in this mode is in order. An instruction word normally contains an 18-bit address field, which is capable of directly addressing 256k of memory. However, in this mode the three most significant bits are used to select the ABR.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.7.5 - contd

This leaves 15 bits of usable address, which are capable of directly addressing 32k of memory. In the formation of the address by the Control Unit the most-significant bit of the remaining 15 (bit 3) is extended into the most-significant three bits of the full 18-bit address (bits 0-2) forming a 2's complement number. This means that if the segment referenced is 256k the low order 16k and the high order 16k can be directly addressed. Any other area of the segment can be addressed only by using an internal base or by address modification. If the segment referenced is less than 240k only the low order 16k can be directly addressed.

If the selected ABR_n is an internal base it must specify another ABR, which is an external base. The external base is selected by bits 18-20 of the internal base. The external base is utilized as described above. The internal base references an address within the segment, and is added to the address formed by the Control Unit. As previously noted the Control Unit extends bit 3 into bits 0-2. This means that the address specified by the internal base can be altered within the range -16k to +16k. In other words think of a segment of memory as being circular in nature, with the maximum size being 256k. The internal base or any address modification moves the 32k block addressable by the instruction word around the circumference of the circle as in the following illustration.



COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

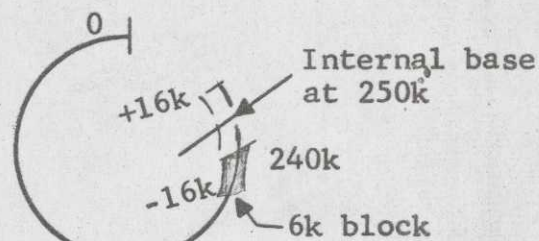
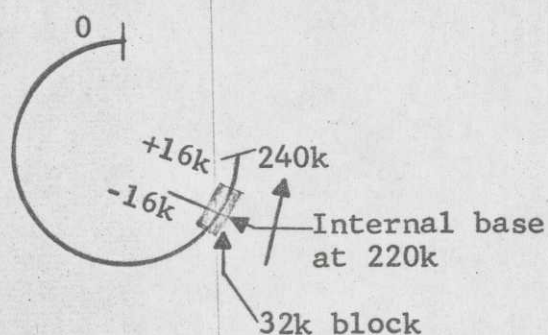
Spec. No. M50EB00107

Cont. on Sh. 2-99 Sh. No. 2-98

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.7.5 - contd

If a segment is not 256k; think of the segment as forming an incomplete circle and it becomes readily apparent that any segment that is less the 256k cannot have its high order 16k directly accessed. If an internal base or address modification is used, the size of the 32k block addressable by the instruction word is gradually reduced as the internal base is moved closer to or greater than the maximum segment size. For example, for a segment of 240k:



No Out Of Bound Fault will occur if the internal base is outside of the segment, since boundary violation is only checked on the final address.

If address modification involving indirection occurs the internal base will be used to obtain the first indirect word, but will not be used again for that instruction.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.7.6 APPENDING CYCLE V (TRANSFER CONTROL TO A NEW SEGMENT)

This cycle is only done during a transfer instruction. It is started by any transfer instruction that actually causes a transfer and has its bit 29 = "1". As in 2.7.5 this will cause an ABR to be selected, which can be either an internal or an external base. The next instruction will be fetched from the address formed by the same method as described in the previous cycle. The contents of the external base, whether selected directly or by the internal base, becomes the new pointer, and is transferred to the PBR. All further memory accesses for operands, indirect words, or instructions will be referenced to the new pointer. If this occurs when the Control Unit is in absolute, the absolute Flag will be reset and the Control Unit will continue in the Appending mode.

2.7.7 APPENDING CYCLE VI (ITS OR ITB ADDRESS MODIFICATION)

During any RI or IR address modification the indirect word may have a tag specifying ITS or ITB modification. Whenever a RI or IR address modification takes place to an even location, two consecutive indirect words are fetched from memory. The first indirect word is inspected to see if calls for ITS or ITB modification. If it does not, the second indirect word is ignored. ITS or ITB modification can take place whether the Control Unit is in Absolute or Append mode. If it is in Absolute and the instruction is not a transfer, the Control Unit will return to Absolute upon completion of the instruction.

2.7.7.1 ITS

Upon detection of an ITS modifier an ITS flag is set, the address field of the first indirect word is transferred to the TBR, and the second indirect word is transferred to the Control Unit as a normal indirect word. A new address is formed by the Control Unit using this indirect word, which may be for another indirect word or for an operand.

COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.2-101 Sh. No.2-100

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.7.7.1 - contd

In either case the ITS flag being set will cause the contents of the TBR to be used as the pointer and Appending will be done using this new pointer. The ITS flag will be reset at the end of that instruction or if an ITB modifier is detected.

2.7.7.2 ITB

Upon detection of an ITB modifier an ITB flag is set, bits 0-2 of the first indirect word are saved, and the second indirect word is transferred to the Control Frame as a normal indirect word. A new address is formed by the Control Frame using this indirect word, which may be for another indirect word or for an operand. In either case the three bits saved select an ABR which can be either external or internal. From this point on the Appending Cycle will be accomplished as described in 2.7.5. The ITB flag will be reset upon receipt of the first operand or indirect word.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.8 INSTRUCTION REPERTOIRE

The instruction repertoire for the GE-645 shall consist of all those 625/635 instructions except for LBAR and SBAR, plus additional instructions to handle the new registers for address appending. Requirements for the new instructions are given in paragraph 3.5.11 of the G.E. 645 ESS. A complete list of all instructions in the repertoire is contained in Appendix A of this specification.

2.9 FAULTS AND EXTERNAL INTERRUPTS

The Processor shall detect illegal operations by the program, faulty communication with memory, programmed faults, and arithmetic faults. It shall react to these faults by forcing the execution of a pair of instructions located at the fault vector. Communication between the Processor and other modules shall be accomplished through the setting and answering of interrupts. For the over-all intermodule communication scheme and the layout of the fault and interrupt vectors see ESS M50EB00105 Section 3.9.

There are 32 faults that constitute the GE-645 fault repertoire. Fourteen of these faults are holdovers from the GE-625/635; the remaining 18 are new. Table 2.9 lists the faults.

The events defined as faults are not necessarily error conditions but may be conditions generated by the program, for example, Timer Run Out, or by an instruction, for example, a call to the Operating System (MME).

Some of the new faults are counterparts of 625/635 faults required for reasons of compatibility, for example, MME, fault tag. Other new faults were dictated by the GE 645 requirements of paging and segmentation, for example, Directed faults.

COMPANY CONFIDENTIAL
 GENERAL ELECTRIC COMPANY
 COMPUTER EQUIPMENT DEPARTMENT
 PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 2-103 Sh. No. 2-102

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Table 2.9 G.E.-645 Faults

Fault Code	Fault Name	Group (Priority)	Change from 625/635 Faults
11110	Startup	I	No Change
11011	Execute	I	No Change
11111	Trouble	II	New
11101	Op Not Completed	II	No Change
11010	Divide Check	III	No Change
11001	Overflow	III	No Change
01100	Parity	IV	No Change
01101	Illegal Memory Command	IV	Modified
11100	Lockup	IV	No Change
01011	Illegal Descriptor	V	New
01010	Illegal Procedure	V	New
01001	635 Compatibility	V	New
11000	635/645 Compatibility	V	New
00001	Master Mode Entry 1	V	No Change
00100	Master Mode Entry 2	V	New
00101	Master Mode Entry 3	V	New
00111	Master Mode Entry 4	V	New
00010	Derail	V	No Change
01000	Fault Tag 1	V	No Change
01110	Fault Tag 2	V	New
01111	Fault Tag 3	V	New
10000	Directed Fault 0	V	New
10001	Directed Fault 1	V	New
10010	Directed Fault 2	V	New
10011	Directed Fault 3	V	New
10100	Directed Fault 4	V	New
10101	Directed Fault 5	V	New
10110	Directed Fault 6	V	New
10111	Directed Fault 7	V	New
00110	Connect	VI	No Change
00011	Timer Runout	VI	No Change
00000	Shutdown	VI	No Change

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.1 FAULT CATEGORIES

There are four general categories of faults. Certain faults may fall under more than one category. The categories and the faults, which may belong to them at one time or another, are as follows:

1) Instruction or program generated -

MME 1-4

DRL

Fault Tag 1-3

Connect

Illegal Procedure

635 Compatability

635/645 Compatability

Timer Runout

Lockup

Overflow

Divide check

Illegal memory command

2) Hardware generated -

Illegal Memory command

Parity

Operation not completed

Trouble

Lockup

3) Manually generated -

Startup

Shutdown

Execute

4) Operating system generated -

Directed faults 0-7

Illegal Descriptor

Trouble

Any instruction or program generated fault caused by the operating system.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.2 FAULT DESCRIPTIONS

1) Startup

A power turn-on has occurred. When the Power On button is depressed the Processor is first initialized and then the Startup fault is recognized.

2) Execute

a) The EXECUTE pushbutton on the Processor maintenance panel has been depressed.

b) An external frequency has been substituted for the EXECUTE pushbutton, for example, scope gate.

The above two are dependent on other maintenance panel switch positions. Also, certain switch positions will affect execution of the instruction set up on the Instruction switches, rather than the fault vector in memory. In either case, the Processor is first initialized and then the Execute fault is recognized.

3) Trouble

The Trouble fault is defined as the occurrence of a fault during the execution of a XED forced by a fault or external interrupt, or during the execution of a SCU which is the first instruction of said XED. Such faults may be hardware generated, for example, operation not complete or parity, or operating system generated, for example, a page containing the indirect address of the SCU is missing.

4) Operation Not Completed

a) The Processor has addressed a Memory Controller to which it is not attached.

b) The addressed Memory Controller failed to acknowledge the Processor.

c) The Processor has not generated a memory access request or a direct operand within 1 to 2 milliseconds and is not in the DIS state.

d) The Memory Controller has closed out a double precision store or a RAR cycle without receiving data from the Processor

e) The Memory Controller failed to acknowledge the data from the Processor during a double precision store or a RAR cycle.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.2 - contd

f) Certain rules specified by the GE-645 Programming Reference Manual were violated causing the Processor to stop and not recognize external interrupts. Examples, DU or DL modifiers with store or RAR instructions; RPD instruction in an even location. Although cases b through e may be attributed to hardware malfunctions, the demonstrated ability of the Processor to carry out the fault sequence tends to indicate that the Processor hardware may not be at fault.

5) Lockup

The Processor is in a program lockup which inhibits recognizing an external interrupt or interrupt type fault for 1 to 2 milliseconds. An example of this condition is the continuous use of the inhibit bit. This is a recoverable fault since the snapshot is valid.

6) Divide Check

A Divide Check fault occurs when the actual division cannot be carried out for one of the reasons specified with each divide instruction.

7) Overflow

An arithmetic overflow, exponent overflow, or exponent underflow has been generated. The generation of this fault is inhibited when the Overflow Mask is in the mask state. Subsequent clearing of the Overflow Mask to the unmasked state will not generate this fault from previously set indicators. The Overflow Fault Mask state does not affect the setting, testing, or storing of indicators. The pinpointing of the type of overflow condition must be done by the control program.

8) Parity

This fault is generated when a parity error exists in a word which is read from a core location:

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.2 - contd

- a) Single precision read - when a single precision word, $C(Y)$, is requested, the contents of the memory pair located at $Y, Y+1$ where Y is even, or $Y-1, Y$ where Y is odd are read from core. The Memory Controller will not report a parity error if it occurs in $C(Y+1)$ or $C(Y-1)$. The pair will be restored with the parity bits unchanged.
- b) Double precision read - when a double precision word, $C(Y, Y+1)$, is requested, the contents of the memory pair located at $Y, Y+1$ are read from core. The Memory Controller will report a parity error if it occurs in either word but no indication is given as to which word it is. The pair will be restored with the parity bits unchanged.
- c) RAR-if a parity error exists in an indirect then tally word, which is to be altered and rewritten, or in an operand for a "to storage" instruction (for example, ASA, ANSA, etc.), the alteration will be carried out and the word will be rewritten in memory with a correct parity bit.

If the parity error occurs on an instruction or an indirect word, the word will not be used any further and the fault routine will be entered. If the parity error occurs on an operand, the Processor operation is completed with the faulty operand before entering the fault routine.

The generation of this fault is inhibited when the Parity Mask indicator is in the mask state. Subsequent clearing of the Parity Mask to the unmasked state will not generate this fault from a previously set Parity Error indicator. The Parity Mask does not affect the setting, or storing of the Parity indicator.

If the parity error occurs on a SDW or PTW, the word will not be used any further and the fault routine will be entered regardless of the state of the Parity Mask indicator.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.2 - contd

9) Illegal Memory Command

The Processor has issued a connect (CIOC) to a channel which is masked off (by program or switch). The Memory Controller will not execute this command. Instead, it will send the applicable illegal action code to the Processor.

The other situations which would potentially cause illegal action responses from the Memory Controller will be trapped by the 635 and the 635/645 Compatibility Faults, or else the restrictions have been removed.

10) Illegal Descriptor

Bits 33-35 of the Page Table Word (PTW), and Segment Descriptor Word (SDW) specify the class of the page or the segment. Five classes (including Directed Fault) have been defined. If the code is detected as one of the three undefined assignments, the Illegal Descriptor fault will be activated.

11) Illegal Procedure

In general, the Illegal Procedure fault is invoked whenever a programming violation is detected whereby one user may adversely affect other users or the operating system. The following subclasses belong under this fault:

- a) GE-645 privileged instructions in Slave mode. The following instructions are covered: LDBR, SDBR, SAM, ZAM, CAM, SCU, RCU, LACL
- b) GE-645 semi-privileged instructions in Slave when the base is locked. The following instructions are covered: EAPn, EABn, TSBn, LDCF, ADBn, LBRn.
- c) Op codes not defined by the GE-645 instruction repertoire including the all zero op code.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 2-109 Sh. No. 2-108

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.2 - contd

- d) An address out of the segment boundary or a pointer out of the descriptor segment boundary.
- e) The location is not to be accessed due to Access bit, Write Permit bit, or Class conventions.

12) GE-635 Compatibility

This fault is intended to trap instructions which appear in the 635 repertoire but not in the 645 repertoire. These instructions are LBAR, SBAR. It will be the responsibility of the operating system to decide on the course of action.

13) GE-635/645 Compatibility

The 635/645 Compatibility Fault is intended to trap all instructions which are privileged in both 635 and 645 repertoires when execution is attempted by Slave procedure. These instructions are SMIC, RMCM, SMCM, CIOC, LDT, DIS and TSS. The last two are not privileged instructions in the 635 but are pointless in Slave mode. It will be the responsibility of the operating system to determine whether the procedure is a 635 Master program running in Slave, or a 635 or a 645 Slave program, and the corresponding course of action.

14-17) Master Mode Entry 1-4

The instruction MME 1-4 has been encountered.

18) Derail

The instruction DRL has been encountered.

19-21) Fault Tag 1-3

Fault tag 1-3 code has been encountered in the tally designator field of an IT address modifier. The indirect cycle will not be made, nor will the operation be completed. Fault tag 1 is reserved for GE-635 programs only. Fault tags 2 and 3 are available to GE-645 programmers. Also fault tags 1, 2 and 3 will be recognized in an IT word brought in by IR modification cycle.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.2 - contd

22-29) Directed Faults

The Directed fault is one of the five classes of segments or pages as defined by bits 33-35 of the Segment Descriptor Word (SDW) or Page Table Word (PTW). Bits 30-32 constitute the number of the Directed fault. The Directed fault is inserted in the SDW or PTW by the operating system to prevent access to the segment or page at this time. Some action by the operating system may be required before the sequence is to be resumed. For example, the page is missing, that is, not in core memory.

30) Connect

The Processor has received a connect pulse from another active device through the Memory Controller. This event is to be distinguished from a CIOC (connect) instruction encountered in the program sequence.

31) Timer Runout

This fault is generated when the contents of the Timer Register reaches zero. If the Processor is in Master mode, recognition of this fault will be delayed until the Processor returns to the Slave mode; this delay does not inhibit the counting in the Timer Register. Since this condition is saved by the hardware, the operating system must exercise care not to transfer it from one user to another.

32) Shutdown

Power will be turned off in approximately one millisecond.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.3 FAULT PRIORITY

Two or more faults may exist in the Processor concurrently due to the "look ahead" feature (that is, overlapping of instruction execution and address preparation). The fault which occurs first through normal program sequence will be serviced. The other fault flags are not safestored and later recognition is contingent on recursion. The only exceptions are Group VI faults which are saved by the hardware for eventual recognition.

The 32 faults are classified into six groups (I-VI) to establish priority when faults occur simultaneously. Group I has the highest priority; Group VI has the lowest. The only exception is the case of a Group III fault (Overflow or Divide Check) caused by an operand having a parity error. In this case the Parity fault (Group IV) will take place.

In the case of simultaneous faults within Group VI, Shutdown has the highest priority, Timer Runout is next, and Connect is the lowest.

No simultaneity of faults within Group V is expected, since they are mutually exclusive. The same is true for faults within Group IV and Group III.

2.9.4 FAULT RECOGNITION

Faults in Group I cause the Processor to initialize and enter the fault routine unconditionally. Op Not Completed cause the Processor to fault unconditionally.

When instructions which may cause Group III faults are executed, the Processor is prevented from going ahead with any irrevocable action. Therefore, if an Overflow or a Divide Check is generated, the Processor is made to halt immediately.

Faults in Group IV cause the operations in the Processor to abort conditionally upon the completion of the operations presently being executed.

Faults in Group V are discovered during the address processing cycle of an instruction. Since this will happen most often in the look ahead mode, the Processor will abort conditionally upon completion of all pending operations. If the execution of any pending instructions causes a fault, it will override the Group V fault.

COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 2-112 Sh. No. 2-111

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.4. - contd

Faults in Groups III-VI must wait for the Memory Controller to acknowledge the last access request before initiating the abort routine.

Faults in Group VI are recognized under similar conditions to External Interrupts. The sampling of any one of these faults may be inhibited in Master mode by the Interrupt Inhibit bit (28). The presence of Group VI faults is normally sampled from the beginning of every address preparation cycle until the generation of the corresponding core location is about to begin. Faults in Group VI have priority over External Interrupts and will cause the operations in the Processor to abort conditionally upon the completion of all pending operations.

2.9.5 FAULT VECTOR ADDRESS

Each fault has a corresponding pair of instructions, known as the Fault Vector pair, to which it is trapped by the hardware. The 32 vector pairs constitute the fault block of 64 words. The base address of the block (as a 0 mod 64 number) is set on 18 switches on the Maintenance Panel or Reconfiguration Console known as the FAULT VECTOR switches. To generate the Fault Vector address, the fault code is extended by a trailing zero (doubled) and concatenated to the value of the FAULT VECTOR switches. The resultant 24-bit number is the core location (absolute address) of the desired Fault Vector pair.

FAULT VECTOR Switches				Fault Code	0
0		17	18	22	23

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.6 FAULT SEQUENCE

Following the detection of a fault condition, the Control Unit will determine the proper time to initiate the fault mode according to the type of fault. At that time the Control Unit takes a snapshot of its status in expectation of the eventual SCU instruction, and then it aborts the whole Processor. At the end of the abort cycle, the address of the Fault Vector pair is prepared. The op code of XED and the Fault Vector pair's address are forced into the Instruction Register and also bit 28 (Interrupt Inhibit) is set to '1' as the Control Unit steps into an address preparation cycle (PA). Since the brute forced XED does not specify any address modification ($t_m = R$, $t_d = N$), the address formed by concatenating the fault code and the FAULT VECTOR switches becomes the core location. The Processor will then issue a memory access request for the vector pair. Also, if the faulting instruction was not an XED'd instruction, then a proper flag (XDE or XDO) must be set to indicate whether it was in an odd or in an even location. This is done to allow the program to return to the next instruction in the sequence in case the fault vector does not transfer. When the Processor enters the XED instruction, it sets a temporary Absolute mode flag not affecting the Absolute indicator. Also, the mode of execution of the XED and the vector pair is set to Master.

If the attempt to execute the XED results in a parity or a Group II fault, the Processor will switch to Trouble fault. The snapshot remains the same, but a new XED instruction is brute forced with an address corresponding to the Trouble fault.

If the execution of the XED is successful, the Control Unit will begin address preparation for the even instruction, which is likely to be a SCU. If it is a SCU, bit 28 should be set to '1' or else external interrupts may be honored and the original snapshot will be destroyed.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.6 - contd

If a Directed fault, Illegal Descriptor, Out of Bounds, or Access Violation fault is encountered during any address preparation cycle for the SCU operand or indirect word; or if a parity follows the fetch of an indirect word, the Trouble fault routine will be entered as discussed previously.

After the first instruction has been completed successfully and did not result in transfer of control, the Processor will begin address preparation for the second instruction. At this time, the Processor is capable of recognizing External Interrupts or faults and recovery. Therefore, the use of bit 28 is optional.

If any of the two instructions results in an actual transfer of control other than TSS, or a transfer with bit 29 = 1, or ITB or ITS indirection, then the Absolute Indicator will be ON. The mode of execution will remain Master unconditionally for as long as the Absolute indicator is ON. If the Absolute indicator is OFF, the mode of execution will be set according to the descriptor of the current procedure.

The two instructions of the Fault Vector must adhere to the programming rules of normal XED.

If neither of the XEDed instructions causes a transfer of control, the hardware will execute the instruction next in normal sequence (ICTC+1) to the instruction which caused the fault directly, or indirectly.

2.9.7 STATUS SAFESTORE AND RESTORE

The information saved by the snapshot following the recognition of faults is intended to be used by the hardware to restore the Processor if and when necessary, and by the software to define the fault and course of action more specifically. The safestored data contains the contents of various registers, status flags and a computed address for a total of three double words (216 bits).

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 2-115Sh. No.2-114

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.7 - contd

A Group V fault is detected during the address preparation cycle which generates it and the Processor is inhibited from advancing to the next cycle. Also, when a Group VI fault is sampled in the beginning of an address preparation cycle, the Processor is not allowed to advance. Therefore, the snapshot taken for a Group V or VI fault captures the precise state of the Control Unit which caused the fault. A Group IV fault is detected after the address preparation cycle that generated it is completed: The Control Unit will be one or two cycles ahead. The Control Unit is not designed to reconstruct the complete snapshot except in lockup. However, the Procedure Base Register (PBR) and the Instruction Counter (ICTC) will point to the faulting instruction.

A Group III fault is detected during the actual execution of the instruction. Again, the snapshot is capable of producing only the PBR and the ICTC which pinpoint the instruction. This is believed to be adequate. A Group I or II fault other than Trouble is brute forced and the snapshot is really immaterial. The snapshot accompanying the Trouble fault is that of the original fault. For more details concerning the information stored by the snapshot see SCU instruction in Appendix A.

There are a number of ways in which the process may be restored, depending on the type of fault or/and the particular application. In some cases, for example, Directed faults, restoration may be achieved by a RCU pointing to the original SCU data. The original sequence will be completed as though the interruption had never occurred. In some cases, for example, Fault Tag 2, the restoration may be achieved by a RCU pointing to modified SCU data. The common feature of both methods is that the return is made to the interrupted instruction. There may be other cases, for example, MME, in which the RCU will point to the next instruction in sequence. Still, in other cases, for example, Execute, the SCU data may be ignored and a transfer will be executed to the desired point.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.7.1 Correlation of Safestore Data with Safestore Status and Faults

This paragraph(s) will be supplied at a later date and will list the conditions for correlating the snapshot of data and status stored by the SCU instruction with specific fault conditions.

2.9.8 ADDRESS AND POINTER GENERATION FOR GROUPS V, VI

A Group V or VI fault is detected during an address preparation cycle and the actual memory fetch is inhibited. However, the cycle will generate an address and a pointer defining the word, whose fetch is being attempted. The computed address and the pointer become part of the safestore. Certain faults may be encountered during any address preparation cycle, for example, Directed faults or access rights violations. Other faults are trapped during the initial address preparation cycle (PA). The following faults fall in this category: 635 Compatibility, 635/645 Compatibility, privileged instructions in Slave mode. A third group of faults is trapped during the effective address preparation cycle. The following faults fall in this category: MME1-4, DRL, semi-privileged instructions in Slave mode contrary to lock bit convention. In all cases, except as noted below, the "computed address" field of the snapshot will contain the address generated by the faulting cycle (BS₀₋₁₇). In the case of Fault Tag 1,2,3 encountered in an indirect word, the "computed address" field of the snapshot will contain the address of the indirect word containing the Fault Tag. The pointer generated by the address preparation cycle will be contained in the "TBR" field of the snapshot.

2.9.9 EXTERNAL INTERRUPTS

In the 600 System, when a device requires a service routine, a request is made to interrupt a current program and engage a Processor in the required task. In this fashion, the system is relieved of the burden of having to continuously test the existence of events requiring attention. Instead, when an event such as the termination of an I/O action takes place it is capable of causing a program interrupt automatically.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.9 - contd

The 600-line Memory Controller has a 32-bit flip-flop register (Execute Interrupt Register) for the purpose of receiving program interrupt requests from active devices associated with it. Each active device is allocated specific cells in the register according to its functional requirements. The cells have a priority hierarchy - cell 0 is assigned the highest priority and cell 31 is the lowest. The active device may set any of the cells allocated to it by issuing a SXC command to the Memory Controller. This command is accompanied by a pattern on data lines 0-15 to be used in selecting interrupt cells. If data line 35 is a 1, the information is applied to cells in the lower half of the register. If data line 35 is a 0, the upper half of the register is selected. When issuing an SXC command, the active device must place a 1 on the protect line, that is, Master mode in the case of a Processor. The Execute Interrupt Register, however, may not be read or reset by programming. The resetting is accomplished following the response by the Processor as will be explained later. This action is wired into the system.

Associated with the Execute Interrupt Register there is in the Memory Controller a 32-bit flip-flop Interrupt Mask Register. There is a bit-to-bit correspondence between the two registers. Interrupt mask cells may be set or reset by the "Control" Processor issuing a SMCM command in the Master mode. The Mask Register will assume the bit configuration of A0-A15 and the Q0-Q15. (Also, the bit configuration of A32-A35 and Q32-Q35 will be imposed on the Channel Interrupt Mask Register.) The designation of "Control" Processor is made by an eight position selector switch located on the Memory Controller Panel. The Control Processor has the ability to read the Mask Register by means of the RCMC command in the Master mode.

When one, or more, of the unmasked execute interrupt cells is set to 1, the Memory Controller places a logical "1" level on the Execute Interrupt Present Line of the "Control" Processor channel. Each execute interrupt cell has an instruction pair associated with it, whose absolute address is a function of the cell number and the Processor Port Number.

COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107 117

Cont. on Sh.2-118 Sh. No. 2-117

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.9 - contd

The first instruction is expected to store the Processor status so that restoration can be made to the point of interruption. The second instruction is expected to cause a transfer to the service routine corresponding to the particular interrupt cell.

The Processor samples periodically the eight Interrupt Present Lines from the Memory Controllers to whom it is connected, and strobes them into its Interrupt Present Register (IPR). If one or more cells of IPR is set, the Processor enter the Prepare Execute Interrupt (PC) cycle. When all operations already in process are completed, and no fault condition is encountered, the Processor issues an Execute Interrupt (XEC) command to the Memory Controller corresponding to the highest priority IPR cell which is on. Since the Processor may be designated "Control" by more than one Memory Controller, the highest priority is assigned to the MC connected to port A, and the lowest to port H. To issue an XEC command the Processor must step into the Master mode.

The Memory Controller verifies that the XEC command was indeed, issued by the "Control" Processor in Master mode. If this is not the case the MC responds with an illegal action code and the Processor traps to the Illegal Memory Command fault. Since the functions involved are wired, rather than programmed, a hardware malfunction should be suspected. If the XEC command is validated, the MC responds by sending the encoded number (5 bits) of the highest unmasked interrupt cell which is set, on data lines 12-16, and resetting this cell. If any other unmasked cell is still set, however, the Interrupt Present Line remains high. The Processor receives the cell number as part of the address of the vector pair. This address is used with a forced XED instruction to retrieve the instruction pair from memory. The interrupt-initiated routine is executed next.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.9.1 External Faults

Three events, which are treated as external faults by the Processor, are sampled at the same time as Execute Interrupts. These are the Connect Pulse, Timer Runout and Power Shutdown. These events are stored in three flip-flops asynchronously as they happen. The outputs of these flip-flops are sampled during Execute Interrupt sampling time and a special flip-flop is set if the Connect or Shutdown flip-flops are set, or if the Timer Runout is set and the Processor is in Slave mode. This flip-flop may be viewed as a member of the IPR and having the highest priority.

2.9.9.2 Interrupt Inhibit Bit

Bit 28 of the instruction word is defined as the interrupt inhibit bit. When the Processor is in Master mode and the current instruction has a 1 in position 28, the recognition of External Interrupts (and External faults) will be inhibited until a subsequent instruction with a 0 in position 28 is encountered, or the Master mode is exited.

The interrupt inhibit bit enables the interrupt-initiated or fault-initiated routine to get started and save certain status of the interrupted program (for example, SCU, STT, RMCN) without being interrupted. At this point, a suitable pattern may be loaded into the Mask Register (SMCM) to prevent interruption by the same cell or cells of lower priority. To be fully effective an SMCM should be issued to all Memory Controllers for whom the interrupted Processor is designated as "Control." Next, the service routine may proceed without the use of the interrupt inhibit bit. Prolonged use of bit 28 to inhibit interrupts is not recommended since fast response to interrupts is vital in real time environments.

2.9.9.3 Lockup Fault

The Lockup fault is recognized when the Processor fails to sample the Interrupt Present Lines for a period of 1-2 milliseconds. The fault may be due to continuous use of bit 28, or a hardware malfunction. The timing is derived from a crystal oscillator and a counter generating a 1 kilocycle pulse train. Since the test involves absolute elapsed

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.9.3 - contd

time rather than Processor execution time, or memory cycles, one should not simply add the execution times of the instructions because the Processor may have to wait for certain memory accesses due to simultaneous requests by the GIOC or the Drum.

The coding of a single instruction with a 0 in bit 28 will cause the Processor to sample the Interrupt Present Lines and reinitiate the lockup test.

The Lockup fault is deactivated during the DIS state.

2.9.9.4 DIS

In the DIS, or initialized state, no operation takes place, and the Processor waits for Execute Interrupt or an External fault signal. The DIS state is entered after the POWER ON button is depressed and the Processor is initialized, or the STOP switch is activated in the test mode, or the system remote stop switch is activated, or a DIS instruction is encountered in the Master mode. When the interrupt or the fault arrives, the Processor generates a strobe IPR pulse and enters a preparation cycle for Execute Interrupt or fault routine.

2.9.9.5 Interrupt Sampling Period

In the GE-645 Prototype Processor the interrupt sampling period takes place in the beginning of every address preparation cycle other than for instruction fetch. This occurs nominally once every 0.750 - 2.250 microseconds. When the current instruction is executed in Master mode and its bit 28 is set to a 1, the strobing of IPR is inhibited. The strobing is also inhibited during multiple-step instructions (for example, LREG, STB) later than the first step.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.9.5 - contd

Due to the look ahead logic, the Processor may be prevented from stepping into a new address preparation cycle until the operation of the one, or two, or three previously prepared operands is completed. The longest waiting time is encountered when two floating-point operations such as DFDV or DFDI are in various stages of execution when the Interrupt Present Line goes high. It may take up to 50 microseconds before the XEC command will be issued to the MC. Furthermore, the arithmetic operation may cause a fault, for example, overflow, and a fault routine will be initiated and recognition of the interrupt will have to be postponed.

The strobing of IPR during interrupt sampling period stops when the interrupt or fault sequence is initiated, and does not resume until the first instruction, whose bit 28 is a 0, is encountered. The hardware forces a 1 in bit 28 of the forced XED instruction, which fetches the interrupt or fault vector. It is the responsibility of the programmer to insert 1's in all programmed instructions which he desires to be interrupt-inhibited. The effect of bit 28 of an XEC or XED does not extend to the XEC'ed or XED'ed instructions. The effect of bit 28, however, is propagated to all subsequent indirect words and operand address preparation cycles even if the latter is a direct operand (DU, DL modification)

2.9.9.6 Address Generation For The Interrupt Vector

There may be up to eight interrupt vector tables for each Processor in a GE-645 Prototype System. Each table is a small block, that is, 64 words which make up the 32 vector pairs. These tables are immediately above, (See fig. 2.9.9.6), the fault vector table of the particular Processor. The tables are relocatable anywhere in the 16M memory by means of 18 FAULT VECTOR switches (F.V.S.). The switches provide the base address, 0 mod 64, of the fault table. The interrupt vector table for the Memory Controller attached to port A is in the next block, the table for port B is in the third block, etc.

COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107 121

Cont. on Sh.2-122 Sh. No. 2-121

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.9.6 - contd

The 18 bit address formed for the forced XED points to the relative location of the vector pair within the Fault Vector. It is added to the Fault Vector Switches (F.V.S.) before addressing memory to form the actual, 24 bit core location in the following fashion:

F.V.S. 0-17 $\xleftarrow{6}$ +EA (effective address of the XED)

The relationship between various ingredients of the address, and the vector tables in core memory is shown in Fig. 2.9.9.6. The least-significant bit of the address of the XED is always 0. The next five bits are the interrupt cell number received from the MC as a result of the XEC command. The next four bits are one of the combinations between 0001 and 1000 (octal 01 and 10) as determined by the label of the port whose Interrupt Present signal is being acknowledged. The eight most significant bits are all zeros.

2.9.9.7 Processor Interrupt Mode

The Processor may enter the interrupt mode of operation when a fault or an Execute Interrupt is recognized and transfer control to a fault-initiated routine or an interrupt initiated routine, respectively. The sequence of events is shown in Fig. 2.9.9.7 and 2.9.9.7a thru d.

Figure 2.9.9.7 outlines the recognition of faults or interrupts. Group VI faults and Execute Interrupts are sampled in the beginning of all operand address preparation cycles for: instruction word (PA); indirect words (PZ); terminating indirect cycle (PN); and indirect then tally word (PT), (if permitted by bit 28). If an Execute Interrupt is present (PC) or a Group VI fault, the cycle is frozen and the next phase will begin when all previously prepared operations have been executed. If no interrupt request is detected, the cycle proceeds and may generate a Group V fault, in which case it is also frozen until all previously prepared operations have been executed.

COMPANY CONFIDENTIAL
 GENERAL ELECTRIC COMPANY
 COMPUTER EQUIPMENT DEPARTMENT
 PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 2-123 Sh. No. 2-122

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

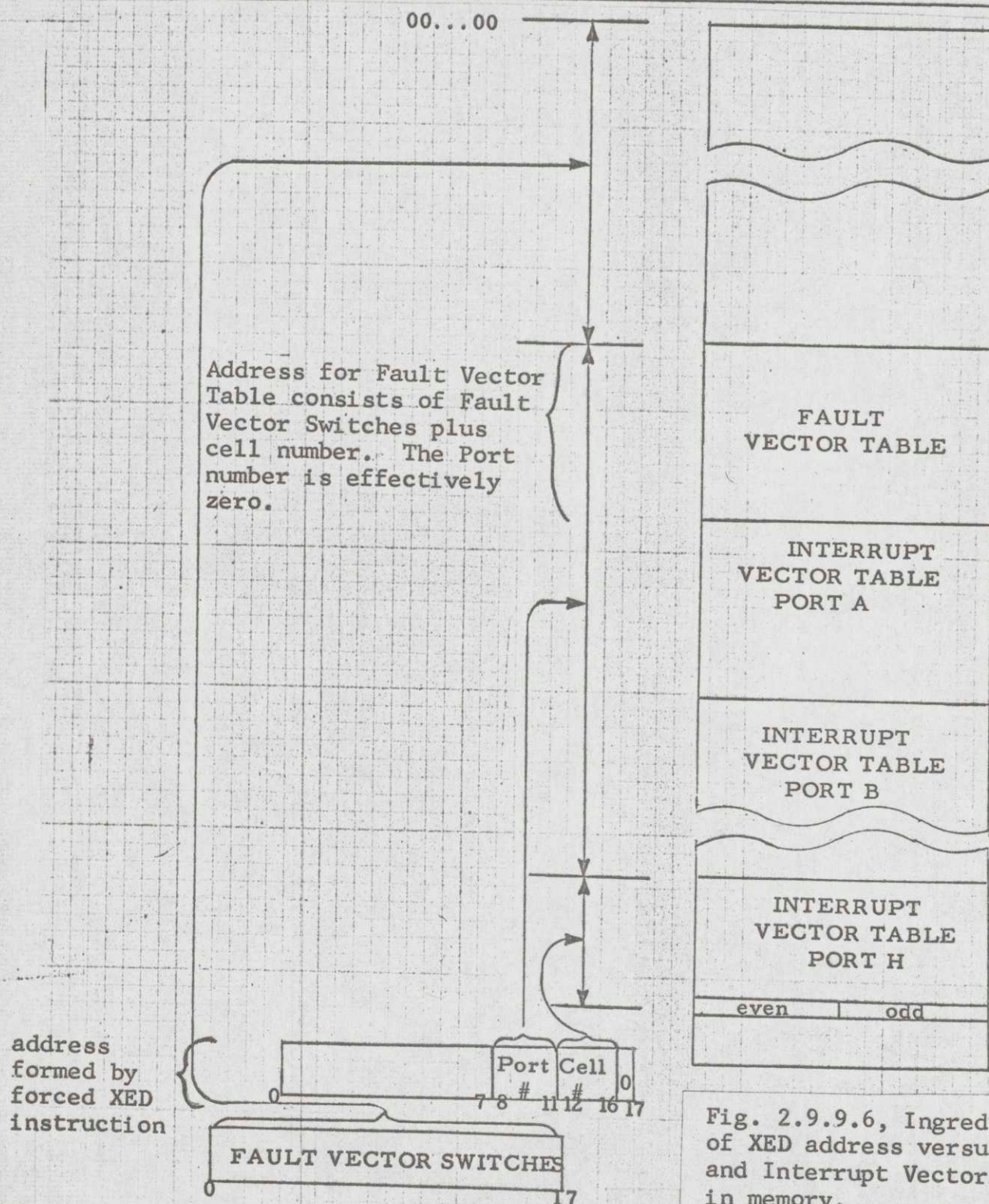


Fig. 2.9.9.6, Ingredients of XED address versus Fault and Interrupt Vector Tables in memory.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 2-124 Sh. No. 2-123

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

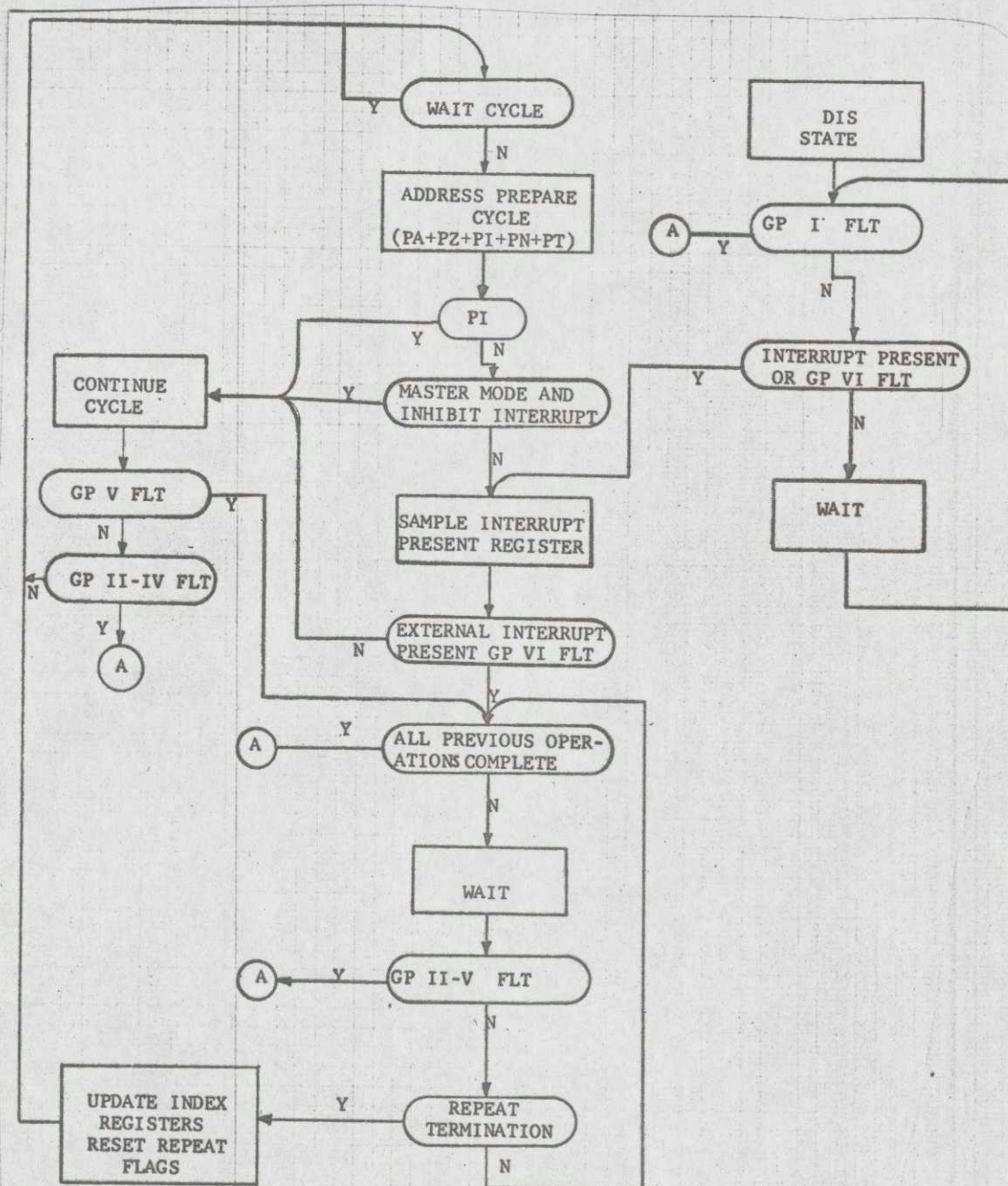


Fig. 2.9.9.7 INTERRUPT MODE FLOW CHART
FAULT OR INTERRUPT RECOGNITION

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 2-125 Sh. No. 2-124

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

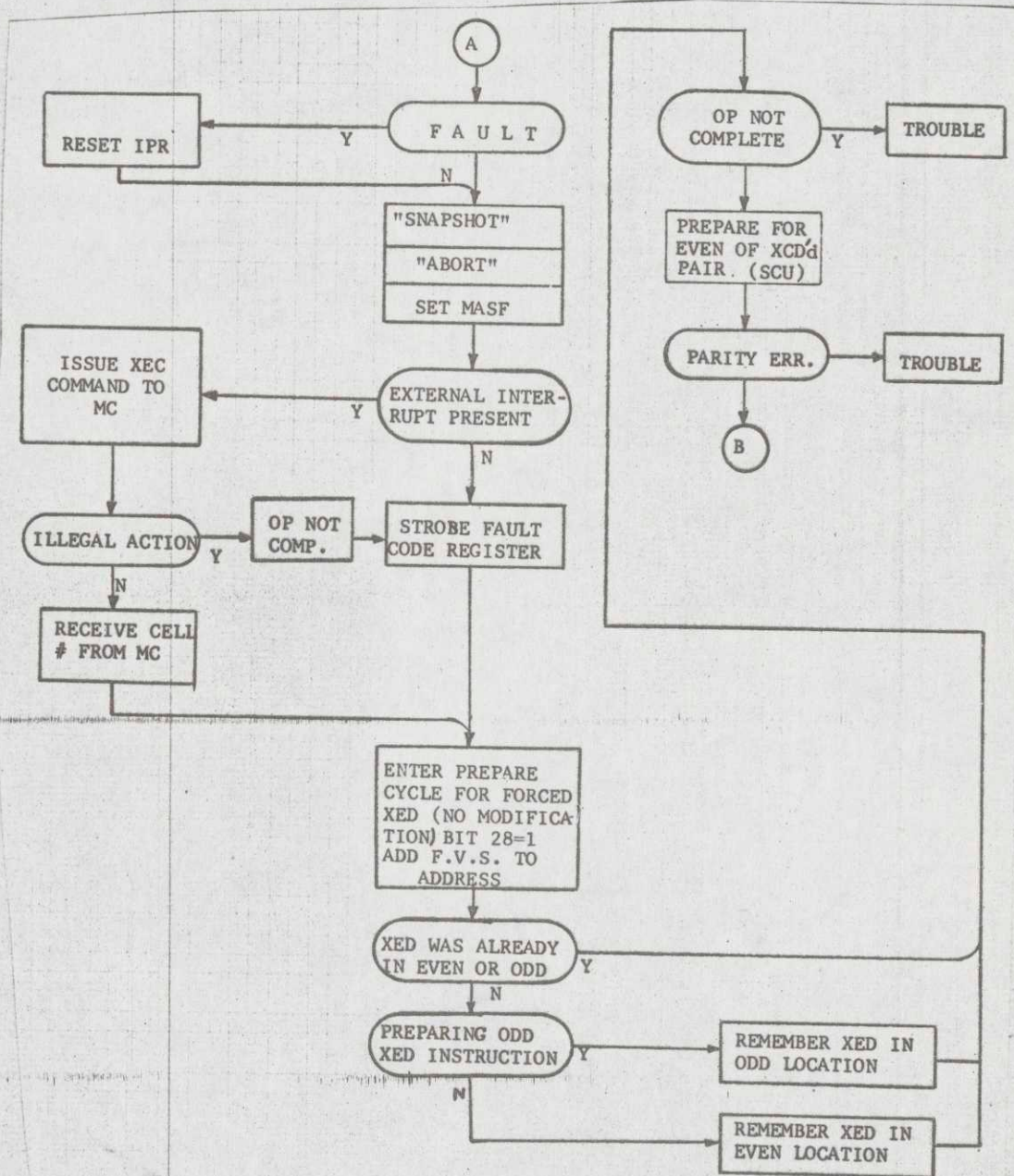


Fig. 2.9.9.7a INTERRUPT MODE FLOW CHART

"SNAPSHOT", ABORT, FORCED XED SEQUENCE

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 2-126

Sh. No. 2-125

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

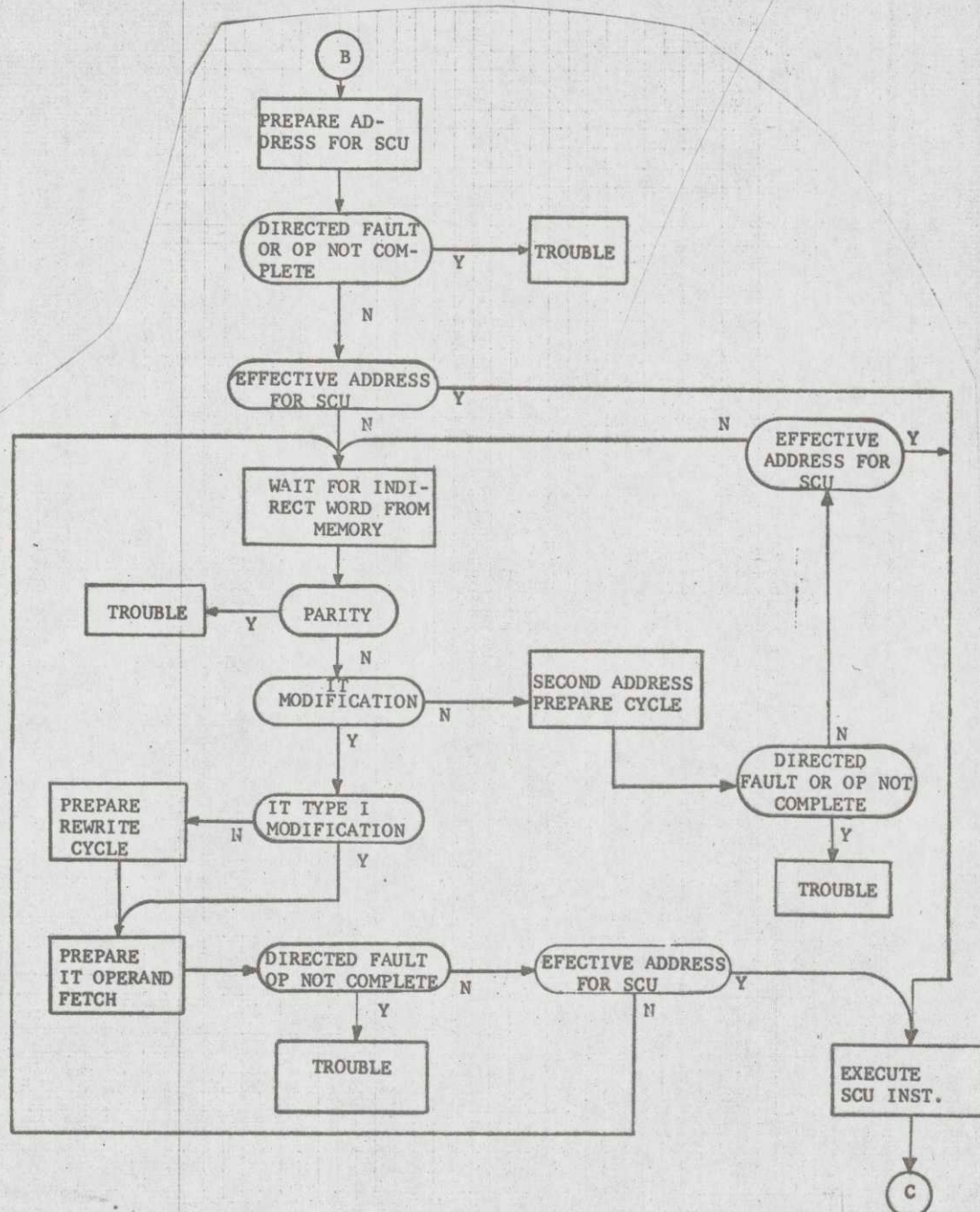


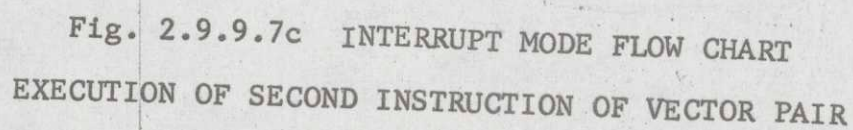
Fig. 2.9.9.7b INTERRUPT MODE FLOW CHART

EXECUTION OF FIRST INSTRUCTION OF VECTOR PAIR

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PHOENIX, ARIZONA

126

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR



TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.9.7 - contd

If no Group V fault is generated, the Processor requests a memory access (except for direct operations). Next, the Processor in some cases has to wait for an indirect word or an XEC'ed or XED'ed instruction; but in most cases another address preparation cycle is initiated. During normal cycles, or when a cycle is frozen, a Group II-IV fault caused by an earlier operation may come up. In this case, the current cycle is abandoned and corrections are made to represent the state of the Processor which caused the fault. Also, it is possible to encounter a termination of "repeat" instruction while waiting for all previously prepared operations to be executed. In this case, the Group V-VI fault or interrupt is ignored; instead, the "repeat" instruction execution will be exited following possible updating of Index Registers. If neither higher priority faults nor "repeat" termination is encountered and all previous operations have been completed, the "snapshot" and "abort" sequence is entered.

Figure 2.9.9.7a shows the "snapshot", "abort" and forced XED sequence. If the sequence is entered due to a fault and an interrupt, the fault takes precedence and IPR is reset. Next, all flags and registers which may be altered before the SCU instruction, must be buffered in "snapshot" registers. The temporary absolute flag, MASF, is set as various flags are initialized during the "abort" phase. The next step is to force an XED instruction without address modifications and with bit 28=1 in the case of a fault, or issue an XEC command to the MC and enter a "Wait for execute address" cycle (WC) in the case of an interrupt. When the cell number is received from the MC then the forced XED is formed and the PA cycle is entered. During this cycle, the address is added to the F.V.S. to form the core location, and if the interruption is not during execution of a normal XED instruction encountered in the program, a flag is set. Also, a flag to detect the Trouble fault is set. The vector pair is now requested from memory.

COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107 128

Cont. on Sh. 2-129 Sh. No. 2-128

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.9.9.7 - contd

The execution of the first instruction is shown in Fig. 2.9.9.7b. The assumption is that the instruction is SCU. During address modifications for the SCU, if a Directed Fault (DIF), Illegal Descriptor, or Out of Bounds is encountered, then the Trouble routine will be entered. This is true if Op Not Complete, Lockup, or Parity in an indirect word is encountered. Upon successful completion of address modification, the SCU is executed by three cycles of double-precision clear-write.

The odd instruction of the vector pair is assumed to be TRA and the flow chart is shown in Fig. 2.9.9.7c. Since the "snapshot" registers have been stored in memory, the Processor is now capable of handling faults without having to define them as Trouble. The exit and return points for faults are shown as S and R, respectively. When the effective address, EA, is generated, the instruction is requested and the address is also strobed into the Instruction Counter (ICTC). If address modifications included bit 29 = 1, or ITB, or ITS, then MASF is reset and the Absolute indicator remains OFF. If the transfer was within the absolute segment, then the Absolute indicator is set ON as MASF is reset.

If the vector pair is not SCU-Transfer, then at Point B, the process is continued according to the XED mode. The presence of a satisfied transfer in either instruction will still cause the Absolute indicator to go ON. However, in the case of Execute Interrupts, Group VI faults, and Directed faults, the vector pair must be SCU-Transfer followed by RCU at the end of the routine, if continuation of the original process as though the interruption had never occurred is to be accomplished.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.10 INSTRUCTION EXECUTION TIMES

This paragraph lists the specifications for instruction execution times that shall be adhered to for the 645 Prototype Processor Module. The actual time for each instruction is also included in the individual instruction descriptions in Appendix A.

2.10.1 BASIS FOR CALCULATION OF THE LISTED EXECUTION TIMES

The listed execution times are the average time for a pair of instructions and are determined from the conditions listed below which are considered the general case.

- 1) The pair is preceded and followed by instructions of the same type.
- 2) The addresses are such that the memory cycles for the preceding instruction fetch and the memory cycles for the operands of the pair are overlapped.
- 3) The address modification is Register Modification (for example R = Xn, AU, etc. but not DU, DL).
- 4) All necessary descriptor words for the appending operation are available in the Associative Memory. In the case of store operations, the "written bit" of the Page Table Word does not have to be set.

The average execution time of an instruction pair, is defined as the time interval between the start of address preparation for the even instruction of the pair, and the start of address preparation for the even instruction of the next pair:

$$\text{Average Execution Time} = \text{Execution Time of Pair} \div 2$$

2.10.1.1 Exceptions to Definition of "Average"

There are five exceptions to the definition of average. The listed execution times reflect these five exceptions. The exceptions are:

- 1) Short Load Type Instructions (for example, LDA, LDAQ, ADA, ADAQ. Any instruction which requires an operand to be loaded from core, and for which the required Operations Unit execution time is less than 1.35 microsecond. When the memory cycle for the preceding instruction fetch, and the memory cycles for the operands of the pair are not overlapped, the execution time for a short load type is 1.5 microseconds.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.10.1.1 - contd

- 2) Store Types (for example, STA, STAQ, FST, DFST, AOS, ASA etc.) - Any instruction which alters the contents of a core location is a store type instruction and the listed execution time specified reflects the following conditions:

- a) The store type instruction is preceded by a short load type instruction (for example, LDA - STA; LDAQ - STAQ; LDA - ASA).
- b) Items 2, 3 and 4 of the general case apply.

The listed execution time is calculated as follows:

$$\text{Store Type Execution Time} = (\text{Execution Time Of Pair}) - (\text{Execution Time Of Load Type})$$

- 3) Long Load Types (for example FAD, FMP, MPS) - Any load type instruction for which the required Operations Unit execution time is greater than 1.35 microseconds. For a string of these instructions, the address preparation time and instruction fetch time is less than the Operations Unit time. The listed execution time is the time interval between the start of the Operations Unit operation for one long load type and the next long load type instruction.
- 4) Control Types (for example, TRA, TNC, XEC) - Any instruction that fetches another instruction to be executed is a control type instruction. The listed execution time is the time interval between the start of address preparation for the control type instruction and the start of address preparation for the next instruction to be executed.
- 5) Base Types (for example, (LBR_n, SBR_n, EAP_n, etc.) - Any instruction which changes or stores a Base Register (ABR 0-7); the Descriptor Segment Base Register or the Associative Memory Registers. The listed execution time is the time interval between the start of address preparation of one base type instruction and the start of address preparation of the next base type; plus, one-half of the instruction address preparation time.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.10.2 ADDRESS MODIFICATION AND APPENDING OPERATION TIMES

The instruction execution time should be increased by the following factors for address modification and appending operations:

- 1) MOD R (R = Xn, AU, etc.): add nothing
- 2) MOD R (R = DU, DL) : add nothing
- 3) MOD IR, RI : add 2 microseconds for each indirection; add 2.3 microseconds for each ITS, ITB indirection.
- 4) MOD IT : add 2 microseconds if the contents of the indirect word are not changed, add 2.7 microseconds if the contents of the indirect word are changed.
- 5) Appending Word Fetch : add 1.6 microseconds for a DSPTW, SDW or PTW fetch.

2.10.3 INSTRUCTION SEQUENCE TIMES

Instruction sequences containing several of the instruction types listed under 2.10.1.1 (exceptions to average execution time) require additional time factors in order that the listed execution times can be used to calculate the actual execution time of the complete sequence. Examples of cases which need additional factors are:

- 1) A transfer to or from a long load type instruction.
- 2) An instruction at location n (n even) modifies and instruction at n + 1, n + 2, n + 3, or an instruction at n (n odd) modifies an instruction at location n + 1, n + 2.
- 3) An instruction at location n (even or odd) modifies a register needed for the address modification of an instruction at location n + 1, n + 2.
- 4) Entry into a fault routine.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107 132

Cont. on Sh.2-133 Sh. No.2-132

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

2.10.4 LIST OF INSTRUCTIONS WITH EXECUTION TIMES

Table 2.10.4 lists the instruction by functional class, the execution times and the exception to the average execution time listed previously as items 1-5 of 2.10.1.1. The times listed are for 50 foot cables between Processor and memory controller.

COMPANY CONFIDENTIAL
 GENERAL ELECTRIC COMPANY
 COMPUTER EQUIPMENT DEPARTMENT
 PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 2-134 Sh. No. 2-133

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

2.10.4 - contd

Table 2.10.4 Instructions By Functional Class With Execution
 Times (50 foot cables)

Instruction		Execution Time (usec)	Exceptions (par. 2.10.1.1)
DATA MOVEMENT			
<u>Load</u>			
EAA	635 Effective Address to Accumulator	1.51	1
EAQ	636 Effective Address to Quotient Register	1.51	1
EAXn	62n Effective Address to Index Register	1.51	1
EABn	(310-313) Effective Address to Base n	1.99	5
EAPn	(330-333) Effective Address to Pair n	2.41	5
LBRn	(350-313) Effective Address to Base n	2.92	5
LDB	76n Load Address Base Register n	6.88	5
LDBR	173 Load Bases	2.92	5
LDCF	232 Load Descriptor Segment Base Register	3.73	5
LDA	512 Load Control Field	1.67	1
LDQ	235 Load Accumulator	1.67	1
LDAQ	236 Load Quotient Register	1.87	1
LDT	237 Load A-Q Register	1.67	1
LDXn	637 Load Timer Register	1.67	1
LXLn	22n Load Index Register n	1.67	1
LDI	72n Load Index Register n from lower	1.67	1
LREG	634 Load Indicator Register	6.29	3
LCA	073 Load Register	1.67	1
LCQ	335 Load Complement into Accumulator	1.67	1
LCAQ	336 Load Complement into Quotient Register	1.87	1
LCXn	337 Load Complement into A-Q Register	1.67	1
	32n Load Complement into Index Register n		

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Store

SAM	557 Store Associative Memory	Note: 29.87-33.33	5
ZAM	157 Store Associative Memory Zero	2.84-6.30	5
SBRn	54n Store Address Base Register n	2.19	5
STB	254 Store Bases	8.25	5
SDBR	154 Store Descriptor Segment Base Register	2.19	5
STPn	(250-253 Store Pair n (650-653))	2.84	5
STCD	357 Store Control Double	2.84	5

Note: The times shown are for absolute and append. SAM and ZAM do not make use of the associative memory for appending since they are used primarily for diagnostic purposes.

STA	755 Store Accumulator	2.08	2
STAC	354 Store A Conditional	3.74	2
STQ	756 Store Quotient Register	2.08	2
STAQ	757 Store A-Q Register	2.61	2
STXn	74n Store Index Register n	2.08	2
SXLn	44n Store Index Register n in Lower	2.08	2
SREG	753 Store Registers	8.59	2
STCA	751 Store Characters of Accumulator (6 bit)	2.08	2
STCQ	752 Store Characters of Quotient Register (6 bit)	2.08	2
STBA	551 Store Characters of Accumulator (9 bit)	2.08	2
STBQ	552 Store Characters of Quotient Register (9 bit)	2.08	2
STI	754 Store Indicator Register	2.47	2
STT	454 Store Timer Register	2.41	2
SCU	657 Store Control Unit	6.44	5
STC1	554 Store Instruction Counter plus 1	2.47	2
STC2	750 Store Instruction Counter plus 2	2.47	2
STZ	450 Store Zero	2.39	2

Shift

ARS	731 Accumulator Right Shift	1.47	3
QRS	732 Quotient Register Right Shift	1.47	3
LRS	733 Long Right Shift	1.47	3

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GENERAL ELECTRIC COMPANY
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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.2-136 Sh. No. 2-135

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

ALS	735 Accumulator Left Shift	1.47	3
QLS	736 Quotient Register Left Shift	1.47	3
LLS	737 Long Left Shift	1.47	3
ARL	771 Accumulator Right Logical	1.47	3
QRL	772 Quotient Register Right Logical	1.47	3
LRL	773 Long Right Logical	1.47	3
ALR	775 Accumulator Left Rotate	1.47	3
QLR	776 Quotient Register Left Rotate	1.47	3
LLR	777 Long Left Rotate	1.47	3

FIXED-POINT ARITHMETIC

Addition

ADBn	(050-053) Add to Address Base Register n (150-153)	3.31	5
ADA	075 Add to Accumulator	1.67	1
ADQ	076 Add to Quotient Register	1.67	1
ADAQ	077 Add to A-Q Register	1.87	1
ADXn	06n Add to Index Register n	1.67	1
ASA	055 Add Stored to Accumulator	3.74	2
ASQ	056 Add Stored to Quotient Register	3.74	2
ASXn	04n Add Stored to Index Register n	3.73	2
ADLA	035 Add Logical to Accumulator	1.67	1
ADLQ	036 Add Logical to Quotient Register	1.67	1
ADLAQ	037 Add Logical to A-Q Register	1.87	1
ADLXn	02n Add Logical to Index Register n	1.67	1
AWCA	071 Add with Carry to Accumulator	1.67	1
AWCQ	072 Add with Carry to Quotient Register	1.67	1
ADL	033 Add Low to A-Q Register	1.67	1
AOS	054 Add One to Storage	3.73	2

Subtraction

SBA	175 Subtract from Accumulator	1.67	1
SBQ	176 Subtract from Quotient Register	1.67	1

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

SBAQ	177 Subtract from A-Q Register	1.87	1
SBXn	16n Subtract from Index Register n	1.67	1
SSA	155 Subtract Stored from Accumulator	3.73	2
SSQ	156 Subtract Stored from Quotient Register	3.74	2
SSXn	14n Subtract Stored from Index Register n	3.74	2
SBLA	135 Subtract Logical from Accumulator	1.67	1
SBLQ	136 Subtract Logical from Quotient Register	1.67	1
SBLAQ	137 Subtract Logical from A-Q Register	1.87	1
SBLXn	12n Subtract Logical from Index Register n	1.67	1
SWCA	171 Subtract with Carry from Accumulator	1.67	1
SWCQ	172 Subtract with Carry from Quotient Register	1.67	1

Multiplication

MPY	402 Multiply Integer	7.09	3
MPF	401 Multiply Fraction	7.09	3

Division

DIV	506 Divide Integer	14.12	3
DVF	507 Divide Fraction	14.12	3

Negate

NEG	531 Negate Accumulator	1.51	1
NEGL	533 Negate Long	1.51	1

FLOATING-POINT OPERATIONS

Load

FLD	431 Floating Load	1.67	1
DFLD	433 Double-Precision Floating Load	1.87	1
LDE	411 Load Exponent Register	1.67	1

Store

FST	455 Floating Store	2.08	2
DFST	457 Double-Precision Floating Store	2.61	2
STE	456 Store Exponent Register	2.08	2

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.2-138 Sh. No.2-137

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Addition

FAD	475 Floating Add	1.99	3
UFA	435 Unnormalized Floating Add	1.99	3
DFAD	477 Double-Precision Floating Add	2.10	3
DUFA	437 Double-Precision Unnormalized Floating Add	2.10	3
ADE	415 Add to Exponent Register	1.67	3

Subtraction

FSB	575 Floating Subtract	2.54	3
UFS	535 Unnormalized Floating Subtract	2.54	3
DFSB	577 Double-Precision Floating Subtract	2.54	3
DUFS	537 Double-Precision Unnormalized Floating Subtract	2.54	3

Multiplication

FMP	461 Floating Multiply	6.04	3
UFM	421 Unnormalized Floating Multiply	5.80	3
DFMP	463 Double-Precision Floating Multiply	11.85	3
DUFM	423 Double-Precision Unnormalized Floating Multiply	11.61	3

Division

FDV	565 Floating Divide	14.52	3
FDI	525 Floating Divide Inverted	14.12	3
DFDV	567 Double-Precision Floating Divide	23.56	3
DFDI	527 Double-Precision Floating Divide Inverted	23.15	3

Negate

FNEG	513 Floating Negate	1.47	3
FNO	573 Floating Normalize	1.47	3

Compare

FCMP	515 Floating Compare	1.79	3
FCMG	425 Floating Compare Magnitude	1.79	3
DFCMP	517 Double-Precision Floating Compare	1.87	3
DFCMG	427 Double-Precision Float. Compare Magnitude	1.87	3
FSZN	430 Floating Set Zero and Negative Indicators from Memory	1.67	1

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 2-139 Sh. No. 2-138

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

BOOLEAN OPERATIONS

AND

ANA	375 AND to Accumulator	1.67	1
ANQ	376 AND to Quotient Register	1.67	1
ANAQ	377 AND to A-Q Register	1.87	1
ANXn	36n AND to Index Register n	1.67	1
ANSA	355 AND to Storage Accumulator	3.73	2
ANSQ	356 AND to Storage Quotient Register	3.73	2
ANSXn	34n AND to Storage Index Register n	3.73	2

OR

ORA	275 OR to Accumulator	1.67	1
ORQ	276 OR to Quotient Register	1.67	1
ORAQ	277 OR to A-Q Register	1.87	1
ORXn	26n OR to Index Register n	1.67	1
ORSA	255 OR to Storage Accumulator	3.73	2
ORSQ	256 OR to Storage Quotient Register	3.73	2
ORSXn	24n OR to Storage Index Register	3.73	2

Exclusive OR

ERA	675 Exclusive OR to Accumulator	1.67	1
ERQ	676 Exclusive OR to Quotient Register	1.67	1
ERAQ	677 Exclusive OR to A-Q Register	1.87	1
ERXn	66n Exclusive OR to Index Register n	1.67	1
ERSA	655 Exclusive OR to Storage Accumulator	3.73	2
ERSQ	656 Exclusive OR to Storage Quotient Register	3.73	2
ERSXn	64n Exclusive OR to Storage Index Register n	3.73	2

COMPARISON

Compare

CMPA	115 Compare with Accumulator	1.67	1
CMPQ	116 Compare with Quotient Register	1.67	1
CMPAQ	117 Compare with A-Q Register	1.87	1
CMPXn	10n Compare with Index Register n	1.67	1

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Spec. No. M50EB00107

Cont. on Sh. 2-140 Sh. No. 2-139

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

CWL	111 Compare with Limits	1.68	1
CMG	405 Compare Magnitude	1.67	1
SZN	234 Set Zero and Negative Indicators from Memory	1.67	1
CMK	211 Compare Masked	1.68	1

Comparative AND

CANA	315 Comparative AND with Accumulator	1.67	1
CANQ	316 Comparative AND with Quotient Register	1.67	1
CANAQ	317 Comparative AND with A-Q Register	1.87	1
CANXn	30n Comparative AND with Index Register n	1.67	1

CONTROL

Transfer

TRA	710 Transfer Unconditionally	2.0	4
TSBn	(270-273) Transfer and Set Base n (570-673)	2.0	5
TSXn	70n Transfer and Set Index Register n	2.0	4
TSS	715 Transfer and Set Slave Indicator	2.0	4
RET	630 Return	4.0	4
RTCD	610 Return Double	3.7	5
RCU	613 Restore Control Unit	4.6	5

Conditional Transfer

TZE	600 Transfer on Zero	2.0	4
TNZ	601 Transfer on NOT Zero	2.0	4
TMI	604 Transfer on Minus	2.0	4
TPL	605 Transfer on Plus	2.0	4
TRC	603 Transfer on Carry	2.0	4
TNC	602 Transfer on No Carry	2.0	4
TOV	617 Transfer on Overflow	2.0	4
TEO	614 Transfer on Exponent Overflow	2.0	4
TEU	615 Transfer on Exponent Underflow	2.0	4
TTF	607 Transfer on Tally-Runout Indicator OFF	2.0	4

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Spec. No. M50EB00107

Cont. on Sh. 3-1 Sh. No. 2-140

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

SPECIAL INSTRUCTIONS

CAM	532 Clear Associative Memory	1.99	5
BCD	505 Binary to Binary-Coded-Decimal	3.71	3
GTB	774 Gray to Binary	9.87	3
CIOC	015 Connect Input/Output Channel	1.35	1
DIS	616 Delay until Interrupt Signal		
DRL	002 Derail	2.0	4
MME	001 Master Mode Entry 1	2.0	4
MME2	004 Master Mode Entry 2	2.0	4
MME3	005 Master Mode Entry 3	2.0	4
MME4	007 Master Mode Entry 4	2.0	4
XEC	716 Execute	2.0	4
XED	717 Execute Double	2.0	4
RMCM	233 Read Memory Controller Mask Registers	1.94	1
SMCM	553 Set Memory Controller Mask Registers	3.97	2
SMIC	451 Set Memory Controller Interrupt Cells	2.0	2
RPT	520 Repeat	1.35	1
RPD	560 Repeat Double	1.35	1
RPL	500 Repeat Link	1.35	1
RSW	231 Read Switches	1.35	1
NOP	011 No Operation	1.47	1
LACL	453 Load Alarm Clock		
RCCL	633 Read Calendar Clock		

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.0 OPERATING INSTRUCTIONS

This section contains the operating instructions for the GE-645 Prototype Processor that may be performed from the operator's Maintenance Panel.

3.1 MAINTENANCE PANEL

The Processor Maintenance Panel may be used by maintenance and operating personnel. All lights and most of the switches are easily accessible. To prevent accidentally altering machine operation the panel has a TEST ENABLE switch that must be activated to place the panel in Test mode. All switches that would adversely affect the operation are either mounted on the back of the panel, or are only active in Test mode.

The Maintenance Panel includes 106 nonswitchable indicators, 180 switchable indicators, 124 two-position toggle switches, 5 three-position toggle switches, 6 pushbutton switches, and 6 rotary switches.

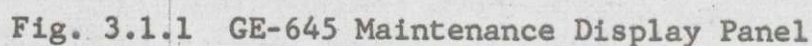
3.1.1 DISPLAY LIGHTS

See Fig. 3.1.1.

Spec. No. M50EB00107

Cont. on Sh. 3-3 Sh. No. 3-2

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR



TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.1.1 Nonswitchable

Miscellaneous

PWR SEQ COMP

When lit it indicates that the power on sequence has completed.

Control Unit Indicators (located in row 1)

HALT

When lit it indicates that:
1) The Processor is in the delay until interrupt mode (DIS).
2) The Processor has stopped running because of the action of the Step Enable switch.

PREPARE FLAGS
(PI,PA,PN,PZ,PT,PC)

These six lights when lit indicate the type of prepare cycle the Control Unit is in.

IC

When lit it indicates that the Control Unit is processing the odd instruction.

B

When lit it indicates that the Control Unit is presenting the odd op code to the Operations Unit.

CFR

When lit it indicates that the Control Frame is ready.

IFR

When lit it indicates that the Interface Frame is ready.

BFR

When lit indicates that the Base Frame is ready.

PIN

When lit indicates that memory has acknowledged a request.

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Spec. No. M50EB00107

Cont. on Sh. 3-5 Sh. No. 3-4

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.1.1 - contd

SDY

When lit indicates that an operand is ready to be sent to memory for a store or the rewrite portion of a RAR.

TMCH
(0,1,2)

These three lights indicate the state of the Too Much Counter.

TG2

When lit indicates that the Control Unit is processing a transfer of control instruction (for example, TRA, TZE, etc.) that is going to transfer.

SRF
(2,3)

These two lights indicate the status of strobe R and strobe down generation.

XDE

When lit indicates that the Control Unit is performing an Execute Double operation from an even location.

SDO XDO

When lit indicates that the Control Unit is performing an Execute Double operation from an odd location.

FR
(0,1)

These two lights indicate the status of the M-register.

MSY

When lit indicates that the instruction pair in the Instruction Register (Y and C) is to be executed in Master mode.

MSI

When lit indicates that the instruction pair in the Instruction Buffer Register (I) are to be executed in Master mode.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.1.1 - contd

ABS

When lit indicates that the current instruction is to be addressed in Absolute mode and executed in Master mode. (Unless bit 29 of instruction word is set to "1" indicating that addressing for the operand is via the Append mode).

Interface Frame Indicators (located in row 2)

ABS

When lit indicates that the current fetch is to be made with an absolute address.

DPT

When lit indicates that a Descriptor Page Table Word is to be fetched.

SDN

When lit indicates that a SDW from a nonpaged descriptor segment is to be fetched.

SDP

When lit indicates that a SDW from a paged descriptor segment is to be fetched.

PTW

When lit indicates that a PTW is to be fetched.

FAP

When lit indicates an indirect instruction or operand word fetch from a paged object segment.

FAN

When lit indicates an indirect instruction or operand word fetch from nonpaged object segment.

SWU

When lit indicates that set written and used bits cycle is in progress.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.1.1 - contd

WBF	When lit indicates that the PTW just received from core memory requires its written bit to be set.
WBS	When lit indicates that the PTW in Associative Memory requires its written bit be set.
AMS	When lit indicates that the address for a fetch is to be formed using a word from the Associative Memory.
LPF	When lit indicates that the fetch is to be made from a large page and when off it indicates that the fetch is to be made from a small page.
CFR	When lit indicates that the Control Frame is ready.
IFR	When lit indicates that the Interface Frame is ready.
BFR	When lit indicates that the Base Frame is ready.
PIN	When lit indicates that memory has acknowledged a request, and the next strobe interrupt may be issued.
DPN	When lit indicates that memory has acknowledged the first half of a double precision or RAR request.
DDA, DAF	Counts strobe DAs for store operations.
WAW	When lit indicates that the Interface Frame is waiting for an appending word from memory.
BIF	When lit indicates that the Processor is executing a Base Frame instruction.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.1.1 - contd

MLS

When lit indicates that the Processor is executing a multiple load or store operation.

MS
(1,2)

Master/Slave mode buffer flip-flops.

TRZ

Indicates the state of the Hold Tally flip-flop. When lit it indicates that the last tally operation changed, or will change the state of the Tally Runout indicator.

DPB, SDB, PTB

These lights indicate the appending state at the time of a Directed, Illegal Class, Out of Bounds, or Appending Parity fault. All these lights are valid only at the time of the fault.

DPB lit indicates that the fault occurred on a DSPTW fetch.

SDB lit indicates that the fault occurred on a SDW fetch from paged or nonpaged descriptor segment.

PTB lit indicates that the fault occurred on a PTW fetch.

APE

When lit indicates that a parity error was detected on an appending word.

Base Frame Indicators (located in rows 1 and 2)

APD

When lit indicates that the Base Frame is doing an appending (PA, PZ, PN, PT cycle) operation.

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Spec. No. M50EB00107

Cont. on Sh. 3-9 Sh. No. 3-8

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.1.1 - contd

WBF	When lit indicates that the Base Frame is waiting for a normal operand.
RWN	When lit indicates that the Control Unit is in a Special WN cycle, where ITS or ITB is possible.
WFM	When lit indicates that the Base Frame is waiting for a possible ITS or ITB modifier.
ITB	When lit indicates that an ITB modifier has been detected.
GBO	When lit indicates that the Base Frame is in its basic timing cycle for general base operations.
IN 0-5	These six lights indicate the state of the Base Increment Counter.

Arithmetic Frame (located in row 3)

SEQUENCE (GS,GF,GO,GD1,GD2 GE, GA, GN, GT)	These nine lights, when lit, indicate the type of cycle the Operations Unit is performing.
FTL	When lit indicates that the Operations Unit is operating in the Repeat Link or Repeat mode.
FRD	When lit indicates that the Operations Unit is operating in the Repeat Double mode.
K (1,2,3)	These three lights indicate the type of operation the S-adder is performing.

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Spec. No. M50EB00107 .

Cont. on Sh. 3-10 Sh. No. 3-9

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.1.1 - contd

Register Frame (located in row 3)

SEQ (GS,GF,GFT,GOM,GC)	These five lights, when lit, indicate the type of cycle the Operations Unit is performing.
ORY	When lit indicates that the Control Unit has placed an op code on the ZOR lines to the Operations Unit.
ORB	When lit indicates that the O-register is busy.
OUB	When lit indicates that the Operations Unit is busy.
YRY	When lit indicates that the Control Unit has placed an operand on the ZDI lines to the Operations Unit.
DDF	When lit indicates that the op code in the O-register has not been decoded.
SDY ₁	When lit indicates that the Operations Unit is performing a fast store operation or a read-alter-rewrite.
SDY ₂	When lit indicates that the Operations Unit is performing a slow store operation.
DIC	When lit indicates that data cannot be placed on the SDI lines.
BCF ₁	When lit indicates that the operand is composed of a 6- or 9-bit character.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.1.1- contd

Associative Memory (located in row 3)

PSH	When lit indicates that a pointer search is in progress.
SDP	When lit indicates that the Associative Memory has found a SDW.
PSL	When lit indicates that a search for a large PTW is in progress.
PSS	When lit indicates that a search for a small PTW is in progress.
SDS	When lit indicates that a SDW search is in progress.
AUV	When lit indicates that an Adjust Usage Counters cycle is in progress.
SCR	When lit indicates that the Adjust Usage Counters cycle has been completed.
REL	When lit indicates that the Interface Frame has finished with the information supplied by the Associative Memory.

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Spec. No. M50EB00107

Cont. on Sh. 3-12 Sh. No. 3-11

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.1.2 Switchable (rows 4-8; See Fig. 3.1.1 and 3.1.2.2)

Rows 4 and 5 (72 indicators) are controlled by the Select 1 switch.

I The I buffer will be displayed. Bits 0-35 in row 4 and bits 36-71 in row 5.

IW1-IW2 The even instruction word (Y-register) will be displayed in row 4. The odd instruction (C-register) will be displayed in row 5.

AQ The A-register will be displayed in row 4. The Q-register will be displayed in row 5.

M The OU-register that receives the operand from memory will be displayed.

H The register that holds the memory operand for the S-adder will be displayed.

N The register that holds the OU operand for the S-adder will be displayed.

S The S-adder output will be displayed.

Row 6 (36 indicators) is controlled by the Select 2 switch.

ICT A-ITC A' Instruction Counter A will be displayed in the 18 indicators labeled SOURCE 1. Instruction Counter A' will be displayed in the 18 indicators labeled SOURCE 2.

ITC C-ITC B Instruction Counter C will be displayed in the 18 indicators labeled SOURCE 1 and Instruction Counter B displayed in SOURCE 2.

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Spec. No. M50EB00107

Cont. on Sh. 3-13 Sh. No. 3-12

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.1.2 - contd

IND-EXP

The 11 indicator flip-flops will be displayed in the indicators as labeled. The floating-point Exponent Register will be displayed in the 10 indicators labeled EXPONENT.

The Indicator register flip-flops will be displayed as follows:

Z = Zero flip-flop
S = Sign flip-flop
C = Carry flip-flop
OF = Overflow flip-flop
EO = Exponent Overflow flip-flop
EU = Exponent Underflow flip-flop
OM = Overflow Mask flip-flop
TR = Tally Runout flip-flop
PE = Parity Error flip-flop
PM = Parity Mask flip-flop

X0 through X7

All even X-registers will be displayed in the 18 indicators labeled SOURCE 1. All odd X-registers will be displayed in the 18 indicators labeled SOURCE 2.

YS-BS

The output of the YS-adder will be displayed in the 18 indicators labeled SOURCE 1. The output of the BS-adder will be displayed in the 18 indicators labeled SOURCE 2.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.1.2 - contd

D-G-O-C

The two Exponent Holding Registers will be displayed in the 8 indicators labeled D and G. The two OU Op Code Registers will be displayed in the 9 indicators labeled O and C.

Z1-Z2-CT
RE-RO

The designated registers will be displayed in the indicators with the corresponding designation.

Row 7 (36 indicators) is controlled by the Select 3 switch.

DSBR-XBI

The Descriptor Segment Base Register will be displayed in indicators 0 through 28. The External Base Identifier will be displayed in the three indicators labeled XBI.

ESTR OSTR ADBRO

The Even and Odd Segment Tag Register will be displayed in the 8 indicators labeled ESTR and OSTR. The Address Base Register 0 will be displayed in indicators 0 through 23.

ADBR 1-7

Address Base Registers 1 through 7 will be displayed in indicators 0 through 23.

FAULT

The indicators labeled F0-F4 display the fault vector. The next nine indicators display the cause of the fault as follows:

FOC - Faulty Op Code
PIF - Privileged Instruction in Slave
LBF - Locked Base Fault
AFL - Appending Fault

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Spec. No. M50EB00107

Cont. on Sh.3-15 Sh. No. 3-14

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.1.2 - contd

OOB - Out of Bounds
PEO - Parity on Operand
PEI - Parity on Instruction (except if to
buffer)
PFI - Parity on Instruction going to
buffer.
PWP - Parity on Appending

Row 8 (36 indicators) is controlled by the Select 4 switch.

PBR-TBR

The Procedure Base Register will be displayed in the indicators labeled PBR. The Temporary Base Register will be displayed in the indicators labeled TBR.

ADR
ZONE-CMD

The Address Register will be displayed in the 24 indicators labeled ADR. The Zone lines will be displayed in the 8 indicators labeled ZONE. The memory command will be displayed in the 4 indicators labeled CMD.

RS

The RS-adder will be displayed in the 18 indicators labeled Address.

DES

The Descriptor Word Register will be displayed.

DOR1

The most-significant 36 bits of the Data Out Buffer will be displayed.

DOR2

The least-significant 36 bits of the Data Out Buffer will be displayed.

DIR-IAL

The DIR1 and DIR2 flip-flops will be displayed in the correspondingly marked indicators. The Illegal Action lines will be displayed in the three indicators labeled IAL.

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Spec. No. M50EB00107

Cont. on Sh. 3-16 Sh. No. 3-15

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.1.2 - contd

ASSOC. MEM UPPER

The most-significant 36 bits of the Associative Memory Data Out lines will be displayed.

ASSOC. MEM LOWER

The least-significant 24 bits of the Associative Memory Data Out lines will be displayed.

NOTE: The data on these Data Out lines will be determined by the ASSOC. MEM BUS SELECT switches. See the description under switches.

3.1.2 SWITCHES

The bulk of the switches are mounted on the front of the panel. There is a switch panel mounted on the back of the main panel, that contains the switches concerned with memory allocation.

3.1.2.1 Switch Descriptions, Switch Panel

See Fig. 3.1.2.1.

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 PHOENIX, ARIZONA

Spec. No. M50EB00107
 Cont. on Sh. 3-17 Sh. No. 3-16

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

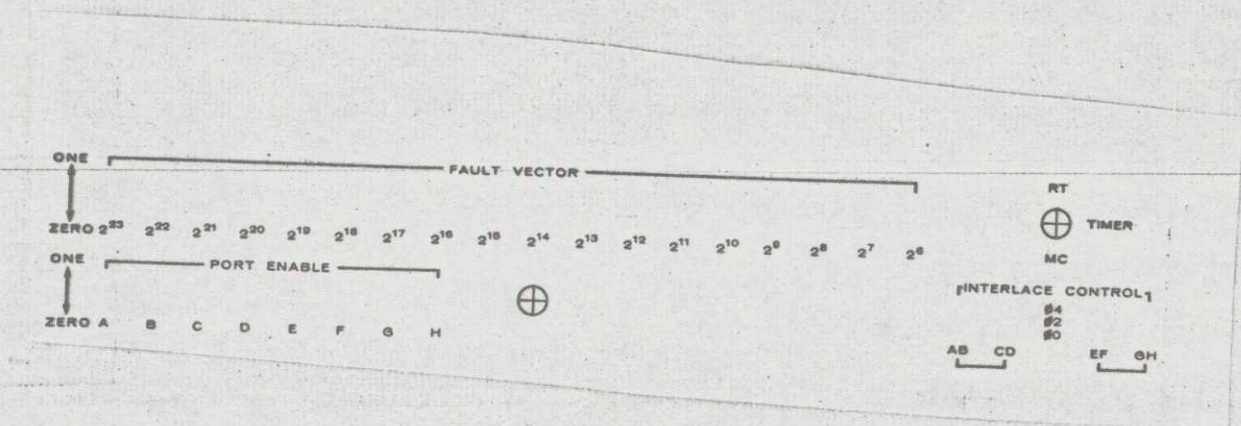


Fig. 3.1.2.1 Switch Panel

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 3-18 Sh. No. 3-17

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.2.1 - contd

FAULT VECTOR

Each of the 32 faults has a corresponding pair of instructions to which it is trapped by the hardware. The 32 pairs constitute a fault block of 64 words. This block is located in memory by the FAULT VECTOR switches, which contain its base address. A fault address is formed by concatenating the 18 FAULT VECTOR switches to the fault code and adding a trailing 0 to form the 24-bit address required.

FAULT VECTOR Switches	Fault Code	0
0 17 18		22 23

PORT ENABLE

There is one toggle switch per memory port. In the ZERO position it turns off the corresponding port by inhibiting the output strobes and the execute interrupts associated with that port.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 3-19 Sh. No. 3-18

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.2.1 - contd

INTERLACE CONTROL

In the GE-645 Memory Controllers can be interlaced in pairs or in groups of four. These switches tell the logic which ports are to be interlaced, and whether it is by two or by four. ($\phi 0, \phi 2, \phi 4$)

TIMER

This switch controls the usage of the Timer Register. When it is in the RT position the Timer Register will be stepped by a 64 kilocycle pulse. When it is in the MC position the Timer Register will be stepped once for each memory cycle.

3.1.2.2 Switch Descriptions, Main Panel

Upper portion of panel. (See Fig. 3.1.2.2.)

POWER ON

Depressing this switch will cause power to be turned on in an orderly fashion.

POWER OFF

Depressing this switch will cause the power to be turned off in an orderly fashion.

SELECT 1, 2, 3, and 4

These switches control the data that will be displayed in the switchable indicators. The exact display is described under the indicators.

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Spec. No. M50EB00107

Cont. on Sh.3-20 Sh. No. 3-19

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

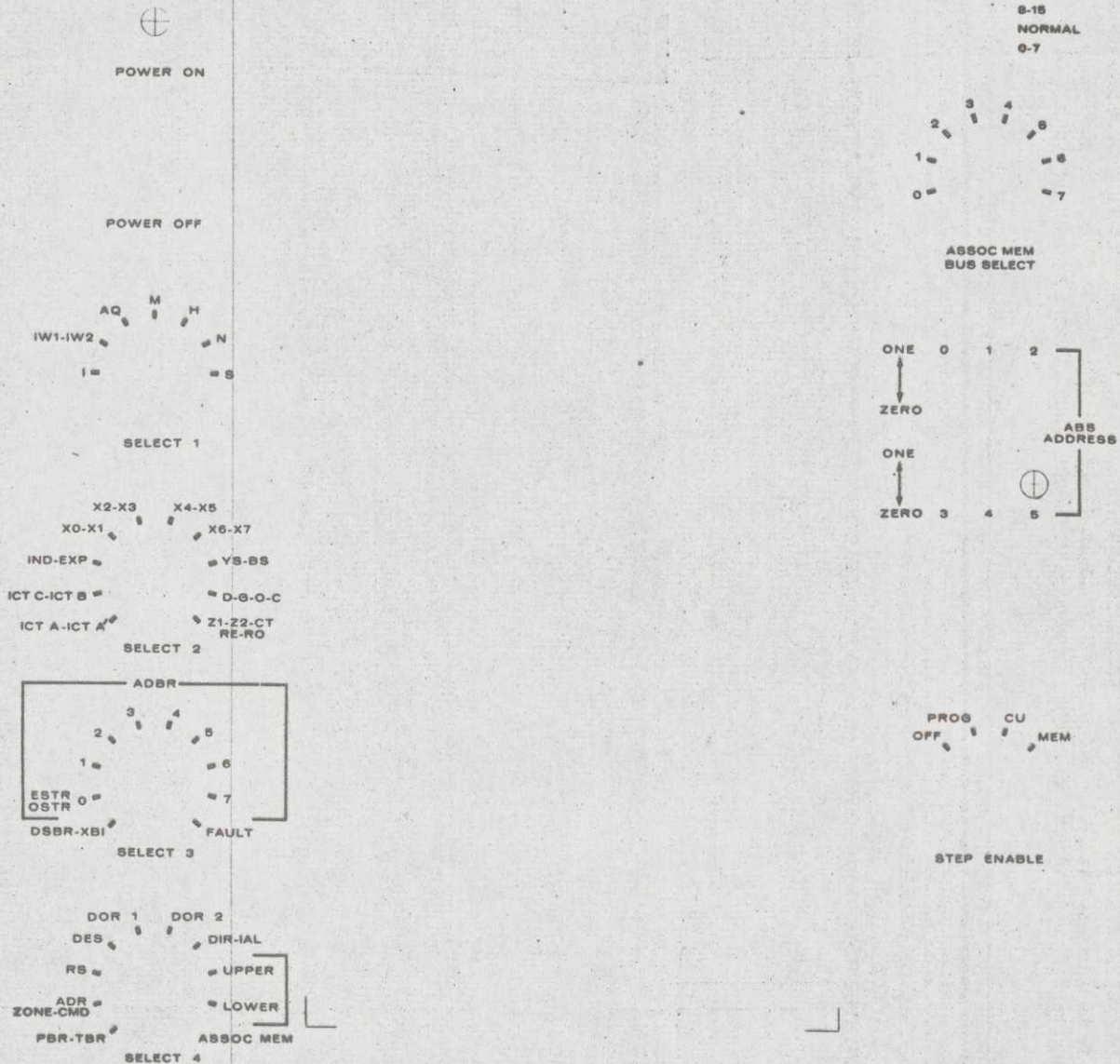


Fig. 3.1.2.2 Top Part of Main Panel

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Spec. No. M50EB00107

Cont. on Sh. 3-21 Sh. No. 3-20

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.2.2 - contd

ASSOC MEM BUS SELECT

These two switches work in conjunction with the Associative Memory display. They are only active under special conditions. The ASSOC MEM OFF switch and the TEST ENABLE switch must be in the TEST position and the Control Unit must not be performing a SAZ or SAM instruction. The three position toggle switch controls the effect of the rotary switch. In the center or NORMAL position the rotary switch has no effect and the normal output of the Associative Memory will be displayed. In the 0-7 position the rotary switch will force the selected Associative Memory Register 0-7 onto the Data Out lines so that it will be displayed. In the 8-15 position the rotary switch will force the selected Associative Memory Register 8-15 onto the Data Out lines.

ABS ADDRESS

These six switches are only used when the Processor is executing the instruction switches in Absolute mode. An absolute address requires 24 bits and the instruction switches have an address field of 18 bits. The six ABS ADDRESS switches form the six most-significant bits of the 24-bit address.

STEP ENABLE

This four-position rotary switch controls the step mode of operation. In the OFF position the Processor will run normally. Moving the switch from OFF to PROG will cause the processor to stop just prior to executing the next PA. Depressing the STEP switch (Fig. 3.1.2.2a) will cause the Processor to execute one instruction and stop. In the CU position the Processor will advance one stroke (\$R) each time the STEP switch is depressed. In the MEM position the Processor will advance one memory cycle each time the STEP switch is depressed. That is, it will go from one \$INT to the next.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh. 3-22 Sh. No. 3-21

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.2.2 - contd

To return to normal operation the STEP ENABLE switch should be returned to OFF and the STEP switch depressed once.

Lower portion of the panel. (See Fig. 3.1.2.2a.)

TEST ENABLE

If this switch is not in the TEST position none of the other switches in that row nor the STEP ENABLE switch will have any effect. When this switch is in the TEST position, besides enabling the other switches, it will light an indicator located just below the STEP ENABLE switch.

STOP ON FAULT

Any one or more of these four switches will, when active, cause the Processor to halt upon recognition of any of the faults associated with that particular switch, and not enter the snapshot/abort sequence. The faults associated with each switch are as follows:

HDW	-	Trouble Parity Illegal Memory Command	}
APD	-	Illegal Procedure Illegal Descriptor Lockup	
PGM	-	MME 1-4 Derail Fault Tag 1-3 Divide Check Overflow 635 Compatibility 635/645 Compatibility	
SOF	-	Directed Fault 0-7	

When any of these switches are activated the op not complete fault is inhibited.

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 PHOENIX, ARIZONA

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Spec. No. M50EB00107
 Cont. on Sh.3-23 Sh. No.3-22

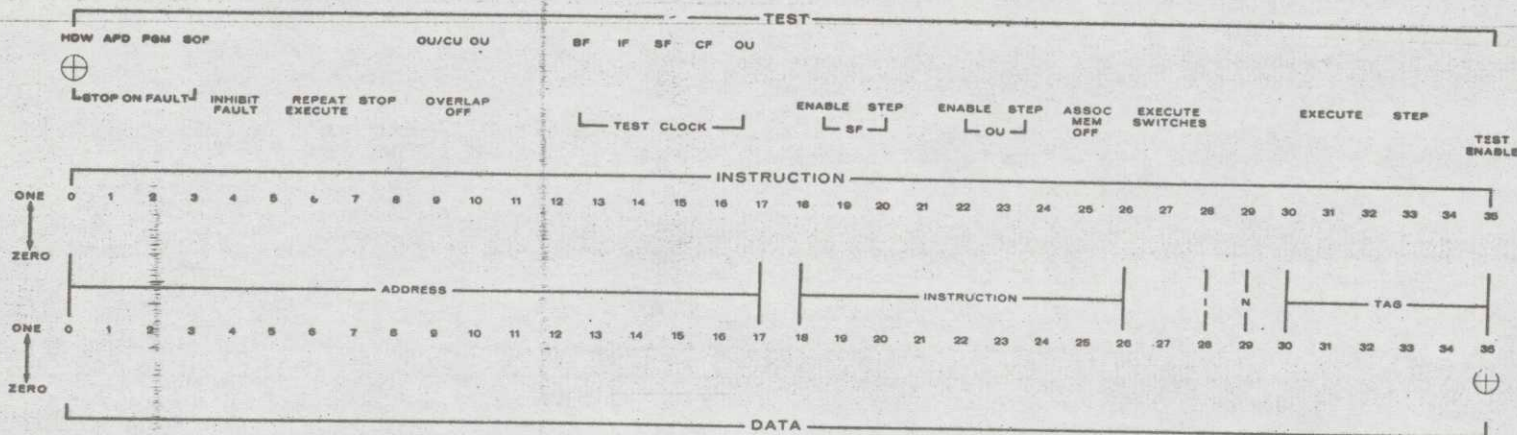


Fig. 3.1.2.2a Bottom Part of Main Panel

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 3-24 Sh. No. 3-23

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.2.2 - contd

To restart the Processor either place the STOP ON FAULT switches in normal or depress the STEP switches.

INHIBIT FAULT

When this switch is active the following faults will not be recognized:

Parity
Connect
Timer Runout
Start Up

REPEAT EXECUTE

This switch when active will allow EXECUTE FAULT or EXECUTE switches operation to be repeated under control of an external sync.

STOP

When this switch is active the Processor will be stopped, initialized, and held in the initialized state. No operation can take place while this switch is active. When it is returned to Normal the Processor will go into a Wait for Interrupt mode (DIS) where it can be started by an Interrupt Signal or by an Execute fault.

OU/CU OVERLAP OFF

When this switch is active the CF will not be allowed to proceed in advance of the OU. The Too Much Counter must equal zero before the CF will prepare an address.

OU OVERLAP OFF

When this switch is active GS will not be allowed to set until GF has reset.

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Spec. No. M50EB00107

Cont. on Sh. 3-25 Sh. No. 3-24

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.2.2 - contd

TEST CLOCK

When any one or more of these switches is in TEST the strobes for the designated frames will be speeded up for marginal testing.

SF ENABLE and STEP

When the ENABLE switch is active the Associative Memory will stop as soon as a search cycle has been initiated. Depressing the STEP switch will generate the next strobe and then stop. Each time the STEP switch is depressed the Associative Memory will advance one strobe time until the search cycle is complete (this may take one, two, or three strobes) and then the Processor will continue until another search cycle is started. To resume normal operation the ENABLE switch must be returned to normal and the STEP switch depressed once.

OU ENABLE and STEP

When this switch is active the OU will stop just prior to issuing a general strobe (\$). Depressing the STEP switch will generate one \$ strobe and then stop. To resume normal operation the ENABLE switch must be returned to normal and the STEP switch depressed once.

ASSOC MEM OFF

This switch when active completely turns off the Associative Memory. It will remain in a stable state until the switch is returned to normal. It is also used to activate the ASSOC MEM BUS SELECT switches.

EXECUTE SWITCHES

If an Execute fault occurs when this switch is active, the data in the Instruction switches will be transferred to both Instruction Registers (Y and C), and that instruction will be executed. An Execute fault can be entered by depressing the EXECUTE pushbutton or by an external sync in REPEAT EXECUTE mode.

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Spec. No. M50EB00107

Cont. on Sh. 4-1 Sh. No. 3-25

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

3.1.2.2 - contd

EXECUTE

Depressing this switch will initiate an Execute fault sequence if the panel is enabled.

STEP

This switch is enabled by the Processor being in a stopped condition. Depressing this switch will generate the necessary strobes to start the Processor. How far it will continue depends upon the setting of the other panel switches. In general the Processor will run until a stop condition, as specified by one of the panel switches, occurs.

DATA SWITCHES

Whenever the Processor executes a "Read Switches Instruction" the contents of these 36 switches will be placed in the A-register. These switches are enabled at all times.

INSTRUCTION

These 36 Instruction switches are placed in both Instruction Registers during an "EXECUTE SWITCHES" operation.

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Spec. No. M50EB00107

Cont. on Sh. 5-1 Sh. No. 4-1

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

4.0 ACCURACY AND RELIABILITY

Accuracy and reliability for the Processor Module shall conform to the specifications outlined in paragraph 3.5.15 and Section 5.0 of the 645 ESS.

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Spec. No. M50EB00107

Cont. on Sh. 6-1 Sh. No. 5-1

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

5.0 INTERFACE REQUIREMENTS

As specified in paragraph 3.5.5 of the 645 ESS, the Processor shall be provided with three types of interfaces.

- 1) Module Interface - for communication with memory modules.
- 2) Remote Configuration Control Interface - for establishing varied combinations of interlace, port and phase selection; both locally and at a remote location with the memory module.
- 3) Operators Console Display - for interface with a remote console, to display significant Processor functions.

Item 1 is covered in detail in paragraph 3.2.1 and Appendix A of the ESS.

Item 2 is covered in detail in paragraph 3.2.4 and Appendix B of the ESS.

Item 3 is covered in detail in paragraph 3.2.5 of the ESS.

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Spec. No. M50EB00107

Cont. on Sh. A1 Sh. No. 6-1

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

6.0 INSTALLATION SHIPPING AND STORAGE REQUIREMENTS

The Processor shall conform to specification M50EB00001
"Common Design Requirements for Computer Department
Products (Rev. A)" with exceptions as noted in
Section 6 of the 645 ESS.

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Spec. No. M50EB00107

Cont. on Sh. A2 Sh. No. A1

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

APPENDIX A INSTRUCTION REPERTOIRE

A 1	Description Format	<u>Page</u> A2	
A 2	Abbreviations and Symbols. . . .	A4	
A 3	Instruction Descriptions	A7	
A 4	Index by Functional Class. . . .	A232	232
A 5	Alphabetical Index	A241	241

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Spec. No. M50EB00107
Cont. on Sh. A3 Sh. No. A2

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

A1 DESCRIPTION FORMAT

A fixed format is used to describe each machine instruction and consists of the following as illustrated by the example below.

<u>Data Movement-Load</u>	
LDA	LOAD ACCUMULATOR
235 ₈	
<u>Summary:</u> $C(Y) \Rightarrow C(A)$	
<u>Description:</u> The contents of the location specified by the absolute address(Y) replace the contents of the Accumulator.	
<u>Modifications:</u> All types	
<u>Timing:</u> 1.67 μ s	
<u>Indicators Affected:</u>	
Zero	If $C(A) = 0$, then ON; otherwise OFF
Negative	If $C(A)_0 = 1$, then ON; otherwise OFF

Headline: The headline identifies the instruction mnemonic, instruction name, and octal operation code.

Summary: The change in the status of the information processing system effected by the execution of the instruction's operation is described in a short and generally symbolic form. If reference is made here to the status of an indicator, then it is the status of the indicator before the operation is executed.

Description: A description of the instruction is included when the Summary is not sufficient for an understanding of the operation.

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Spec. No. M50EB00107

Cont. on Sh. A4 Sh. No. A3

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Modifications: The modifications listed here are permitted with this instruction. Any exceptions listed shall not be used either because they are not permitted with this instruction or because their effect cannot be predicted from the general address modification procedure.

Timing: This entry lists the instruction execution time based on the conditions explained under the Calculation of Instruction Execution Times discussion in paragraph 2.10 and the exceptions in paragraph 2.10.1.1.

Indicators Affected: The indicators listed are only those indicators whose status can be changed by the execution of this instruction. In most cases a condition for setting ON as well as one for setting OFF is stated. If only one of the two is stated, then this indicator remains unchanged unless the stated condition is met. Unless explicitly stated otherwise, the conditions refer to the contents of registers, etc. as existing after the execution of the instructions operation.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

A2 ABBREVIATIONS AND SYMBOLS

The following abbreviations and symbols will be used for the description of the instructions and subsequent machine operations.

Registers:

A = Accumulator Register (36 bits)
ABR = Address Base Register (24 bits)
AM = Associative Memory (16 registers of 60 bits per register)
AQ = Combined Accumulator-Quotient Register (72 bits)
AR = Associative Register (60 bits)
DSBR = Descriptor Segment Base Register (29 bits)
E = Exponent Register (8-bits)
EAQ = Combined Exponent - Accumulator-Quotient Register (8+72 bits)
ICTC = Instruction Counter (18 bits)
IR = Indicator Register (18 bits, 11 of which are used at this time)
PBR = Procedure Base Register (18 bits)
Q = Quotient Register (36 bits)
TBR = Temporary Base Register (18 bits)
TR = Timer Register (24 bits)
Z = Temporary Pseudo result of a non-store comparative operation.
Xn = Index Register n ($n = 0, 1, \dots, 7$)

Register Positions and Contents:

("R" standing for any of the registers listed above as well as for a memory location or a pair of memory locations.)

R_i = the i^{th} position of R
 R_{i-j} = the positions i through j of R
 $C(R)$ = the contents of the full register R
 $C(R)_i$ = the contents of the i^{th} position of R
 $C(R)_{i-j}$ = the contents of the positions i through j of R

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

When the description of an instruction states a change only for a part of a register or memory location then it is always understood that the part of the register or memory location which is not mentioned remains unchanged.

Absolute Address and Memory Locations:

Y = the absolute address (24 bits specifying the core location) in memory.

Y-pair = a symbol denoting that the absolute address Y designates a pair of memory locations with successive addresses, the smaller address being even. When the absolute address is even, then it designates the pair Y(even), Y+1 and when it is odd, then the pair Y-1, Y(odd). In any case the memory location with the smaller (even) address contains the most significant part of a double-precision number or the first of a pair of instructions.

EA = Effective address. - an 18-bit intermediate operand address containing a segment address. EA is composed of: the address field of the instruction word; an internal base (if designated by bit 29 of the instruction word); any address modification employed prior to a final operand fetch.

Other Symbols:

P = Pointer
⇒ = replaces
∴ = compare with
AND = the Boolean connective AND(Symbol . or ^)
OR = the Boolean connective OR(Symbol = or V)
≠ = the Boolean connective NON-EQUIVALENCE (or EXCLUSIVE OR)
- = minus
+ = plus

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. A7 Sh. No. A6

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

It is a characteristic feature of the GE-645, that an address translation takes place with each memory access unless the Processor is in Absolute mode. The descriptions of the individual machine instructions do not mention the address translation. It is understood that an address translation has to be performed immediately prior to each memory access request regardless of whether:

- The program address is an instruction address, and the memory is accessed for fetching an instruction.
- The program address is a tentative address, and the memory is accessed for fetching an indirect word.
- The program address is an effective address, and the memory is accessed for obtaining an operand or for storing a result.

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Spec. No. M50Eb00107

Cont. on Sh. A8 Sh. No. A7

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

A3 INSTRUCTION DESCRIPTIONS

The complete GE-645 Instruction repertoire is listed by functional order in the following pages.

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Spec. No. M50EB00107

Cont. on Sh. A9 Sh. No. A8

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Load

EAA

EFFECTIVE ADDRESS to ACCUMULATOR

635₈

Summary: $EA \Rightarrow C(A)_{0-17}; 00...0 \Rightarrow C(A)_{18-35}$

Description:

Modifications: All except DU, DL.

Timing: 1.51 μ sec

Indicators Affected:

Zero	If $C(A) = 0$, then ON; otherwise OFF
Negative	If $C(A)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A10 Sh. No. A9

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Load

EAQ EFFECTIVE ADDRESS to QUOTIENT REGISTER 6368

Summary: EA $\Rightarrow$ C(Q)₀₋₁₇; 00...0 $\Rightarrow$ C(Q)₁₈₋₃₅

Description:

Modifications: All except DU, DL.

Timing: 1.51 μ sec

Indicators Affected:

Zero	If C(Q) = 0, then ON; otherwise OFF
Negative	If C(Q) ₀ = 1, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A11 Sh. No. A10

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Load

EAXn EFFECTIVE ADDRESS to INDEX REGISTER n ($n=0, \dots, 7$) $62n_8$

Summary: $EA \Rightarrow C(Xn)$

Description:

Modifications: All except DU, DL.

Timing: 1.51 μ sec

Indicators Affected:

Zero	If $C(Xn) = 0$, then ON; otherwise OFF
Negative	If $C(Xn)_0 = 1$, then ON; otherwise OFF

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. A12 Sh. No. A11

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Data Movement-Load
EABn	EFFECTIVE ADDRESS to BASE n (n=0, 1, ..., 7)	310-313 330-333 ₈

Summary: $EA \Rightarrow C(ABRn)_{0-17}$; $C(ABRn)_{18-23}$ are unchanged, and any associated external base designated by $C(ABRn)_{18-20}$ is unchanged.

Description: This instruction may be executed in Master or Slave mode. If attempted in Slave mode an Illegal Procedure Fault will occur unless $C(ABRn)_{22} = 0$.

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 1.99 usec

Indicators Affected: None

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. A13 Sh. No. A12

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Load

EAPn	EFFECTIVE ADDRESS to PAIR n(N=0, 1, ..., 7)	350-353 370-373 ₈
------	---	---------------------------------

Summary: 1) $EA \Rightarrow C(ABRn)_{0-17}; P \Rightarrow C(ABRm)_{0-17}$ if $C(ABRn)_{21} = 0$
2) $P \Rightarrow C(ABRm)_{0-17}$ if $C(ABRn)_{21} = 1$

Where n and m are the designated internal and the linked external ABRs respectively, unless n designates an external ABR.

Description: The effective address EA replaces the contents of the internal ABR(n) designated by the EAPn instruction, (when $C(ABRn)_{21} = 0$), and the Pointer (P) generated as part of the address modification procedure replaces the contents of the associated external ABR(m); m being specified by $C(ABRn)_{18-20}$. If the base specified by the EAPn instruction is external, that is, $C(ABRn)_{21} = 1$, then only $P \Rightarrow C(ABRn)_{0-17}$ takes place. This instruction may be executed in Master or Slave mode. If attempted in Slave mode an Illegal Procedure Fault is generated unless $C(ABRn,m)_{22} = 0$.

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 2.41 μ sec

Indicators Affected: None

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Spec. No. M50EB00107
Cont. on Sh. A14 Sh. No. A13

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Load

LBRn	LOAD ADDRESS BASE REGISTER n (n=0,1,..., 7)	76n ₈
------	---	------------------

Summary: $C(Y)_{0-23} \Rightarrow C(ABRn)$

Description: This instruction may be executed in Master or Slave mode. If attempted in Slave mode an Illegal Procedure fault is generated unless $C(ABRn)_{22} = 0$. The $C(ABRn)_{22}$ is not altered in Slave mode.

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 2.92 μ sec

Indicators Affected: None

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Spec. No. M50EB00107
Cont. on Sh. A15 Sh. No. A14

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Data Movement-Load
LDB	LOAD BASES	173 ₈

Summary: $C(Y, Y+1, \dots, Y+7)_{0-23} \Rightarrow C(ABR0, \dots, ABR7)$

where Y must be an 0 modulo 8 address.

Description: The eight ABR's are loaded in sequence in double-word loads. The contents of the affected ABR may be altered in Master or Slave mode if $C(ABRn)_{22} = 0$. However, the ABR will not be affected and no fault will occur while executing LDB in Slave mode if $C(ABRn)_{22} = 1$.

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 6.88 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A16 Sh. No. A15

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Load

LDBR	LOAD DESCRIPTOR SEGMENT BASE REGISTER	232 ₈
------	---------------------------------------	------------------

Summary: $C(Y)_{0-28} \Rightarrow C(DSBR)$

Description: This instruction may be executed only in Master mode or a fault will occur and C(DSBR) remain unchanged. The Associative Memory is cleared (bit 54 of all AR's set to zero) when LDBR is executed.

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 2.92 μ sec

Indicators Affected: None

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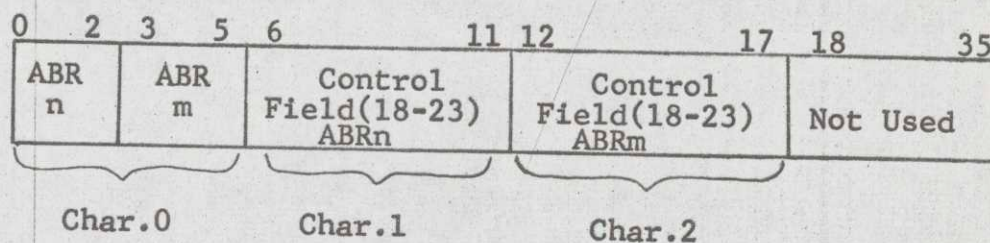
Cont. on Sh. A17 Sh. No. A16

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

LDCF LOAD CONTROL FIELD 512₈

Summary: $C(Y)_{6-11} \Rightarrow C(ABRn)_{18-23}$; $C(Y)_{12-17} \Rightarrow C(ABRm)_{18-23}$
 where n and m are internal and associated external
 ABR's specified by $C(Y)_{0-2}$ and $C(Y)_{3-5}$ respectively.

Description: The $C(Y)_{0-17}$ is interpreted as three 6-bit characters
 specifying two ABR's and the corresponding new ABR
 control field information. This instruction may be
 executed in Master or Slave mode. If attempted in
 Slave mode an Illegal Procedure Fault is generated
 unless $C(ABRn,m)_{22} = 0$. The $C(ABRn,m)_{22}$ is not
 altered in Slave mode. Format of $C(Y)$ is as follows:



Modifications: All types except CI, SC, SCR.

Timing: 3.73 μ sec

Indicators Affected: None

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Spec. No. M50EB00107
Cont. on Sh. A18 Sh. No. A17

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Load

LDA	LOAD ACCUMULATOR	2358
-----	------------------	------

Summary: $C(Y) \Rightarrow C(A)_{0-35}$

Description:

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(A) = 0$, then ON; otherwise OFF
Negative	If $C(A)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A19 Sh. No. A18

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

LDQ	LOAD QUOTIENT REGISTER	Data Movement-Load 236 ₈
-----	------------------------	--

Summary: $C(Y) \Rightarrow C(Q)_{0-35}$

Description:

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Q) = 0$, then ON; otherwise OFF
Negative	If $C(Q)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A20 Sh. No. A19

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Load

LDAQ LOAD A-Q REGISTERS

2378

Summary: C(Y-pair) $\Rightarrow$ C(AQ)

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.87 μ sec

Indicators Affected:

Zero	If C(AQ) = 0, then ON; otherwise OFF
Negative	If C(AQ) ₀ = 1, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A21 Sh. No. A20

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

LDT	LOAD TIMER REGISTER	Data Movement-Load
		637 ₈

Summary: $C(Y)_{0-23} \Rightarrow C(TR)$

Description: This instruction can be used in Master mode only. If its use is attempted in the Slave mode, it generates a 635/645 Compatibility Fault.

Modifications: All except CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(TR) = 0$, then ON; otherwise OFF
Negative	If $C(TR)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh.A22 Sh. No. A21

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Load

LDXn LOAD INDEX REGISTER n ($n=0,1,\dots,7$) 22n₈

Summary: $C(Y)_{0-17} \Rightarrow C(Xn)$

Description:

Modifications: All except CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Xn) = 0$, then ON; otherwise OFF
Negative	If $C(Xn)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A23 Sh. No. A22

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Load

LXLn LOAD INDEX REGISTER n from LOWER (n=0,1,...,7) 72ng

Summary: $C(Y)_{18-35} \Rightarrow C(Xn)$

Description:

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Xn) = 0$, then ON; otherwise OFF
Negative	If $C(Xn)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107
Cont. on Sh. A24 Sh. No. A23

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Load

LDI LOAD INDICATOR REGISTER 634₈

Summary: $C(Y)_{18-27} \Rightarrow C(IR)$ (absolute Mode Indicator $C(Y)_{28}$ not affected)

Description: The relationship between $C(Y)_{18-27}$ and the indicators is as follows:

<u>Bit Position C(Y)</u>	<u>Indicator</u>
18	Zero
19	Negative
20	Carry
21	Overflow
22	Exponent Overflow
23	Exponent Underflow
24	Overflow Mask
25	Tally Runout
26	Parity Error
27	Parity Mask
28	Absolute Mode (Not affected)

Modifications: All except CI, SC, SCR.
The tally runout indicator will reflect $C(Y)_{25}$ regardless of what address modification is performed on the LDI instruction for tally operations.

Timing: 1.67 μ sec

Indicators Affected:

Absolute Mode	Not Affected
All other Indicators	If corresponding bit in C(Y) is ONE, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A25 Sh. No. A24

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Data Movement-Load
LREG	LOAD REGISTERS	073 ₈

Summary: $C(Y, Y+1, \dots, Y+6) \Rightarrow C(X_0, X_1, \dots, X_7, A, Q, E)$; $C(Y+7)$ is not used; where Y must be a 0 modulo 8 address since Y_{15-17} is increased from 000 for location Y, to 111 for location $Y+7$ (four double-length words are pulled from memory).

Description: The contents of the location specified by Y through $Y+6$ replace the contents of the Index (X_0-X_7), A-, Q-, and E-, registers as specified below:

$C(Y)_{0-17, 18-35} \Rightarrow C(X_0, X_1)$ $C(Y+4)_{0-35} \Rightarrow C(A)$

$C(Y+1)_{0-17, 18-35} \Rightarrow C(X_2, X_3)$ $C(Y+5)_{0-35} \Rightarrow C(Q)$

$C(Y+2)_{0-17, 18-35} \Rightarrow C(X_4, X_5)$ $C(Y+6)_{0-7} \Rightarrow C(E)$

$C(Y+3)_{0-17, 18-35} \Rightarrow C(X_6, X_7)$ $C(Y+7)$ is not used

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 6.29 μ sec

Indicators Affected: None

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Spec. No. M50EB00107
Cont. on Sh. A26 Sh. No. A25

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Data Movement-Load
LCA	LOAD COMPLEMENT into ACCUMULATOR	335 ₈

Summary: $-C(Y) \Rightarrow C(A)$ if $C(Y) \neq 0$
 $C(Y) \Rightarrow C(A)$ if $C(Y) = 0$

Description: The contents specified by location Y are negated by forming the 2's complement of the 36-bit number before moving to the Accumulator. If $C(Y)=0$, then no complementing takes place.

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(A) = 0$, then ON; otherwise OFF
Negative	If $C(A)_0 = 1$, then ON; otherwise OFF
Overflow	If range of A is exceeded, then ON

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Spec. No. M50EB00107

Cont. on Sh. A27 Sh. No. A26

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Load

LCQ LOAD COMPLEMENT into QUOTIENT REGISTER 336₈

Summary: $-C(Y) \Rightarrow C(Q)$ for $C(Y) \neq 0$

$C(Y) \Rightarrow C(Q)$ for $C(Y) = 0$

Description: The contents of the location specified by Y are negated by forming the 2's complement of the 36-bit number before moving it to the Q-register. If $C(Y) = 0$, the number is moved to the Q-register without complementing.

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Q) = 0$, then ON; otherwise OFF
Negative	If $C(Q)_0 = 1$, then ON; otherwise OFF
Overflow	If range of Q is exceeded, then ON

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Spec. No.M50EB00107

Cont. on Sh. A28 Sh. No. A27

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Data Movement-Load
LCAQ	LOAD COMPLEMENT	into A-Q REGISTER
		337 ₈

Summary: $\neg C(Y\text{-pair}) \Rightarrow C(AQ)$ if $C(Y\text{-pair}) \neq 0$
 $C(Y\text{-pair}) \Rightarrow C(AQ)$ if $C(Y\text{-pair}) = 0$

Description: The contents of the locations specified by the Y-pair are negated by forming the 2's complement of the 72 bits while moving it from the locations specified by the Y-pair to the combined A-Q-registers. If the $C(Y\text{-pair}) = 0$, the number is moved to the A-Q-registers without complementing.

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.87 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF
Overflow	If range of AQ is exceeded, then ON

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Spec. No. M50EB00107

Cont. on Sh.A29 Sh. No.A28

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Load

LCXn LOAD COMPLEMENT into INDEX REGISTER n ($n=0,1,\dots,7$) 32n₈

Summary: $-C(Y)_{0-17} \Rightarrow C(Xn)$ for $C(Y) \neq 0$

$C(Y)_{0-17} \Rightarrow C(Xn)$ for $C(Y) = 0$

Description: Bits 0-17 of the contents of the location specified by Y are negated by forming the 2's complement of the number contained in Y while moving to the Index Register specified. If $C(Y)_{0-17} = 0$, then the 18 bits are moved without complementing.

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Xn) = 0$, then ON; otherwise OFF
Negative	If $C(Xn)_0 = 1$, then ON; otherwise OFF
Overflow	If range of Xn is exceeded, then ON

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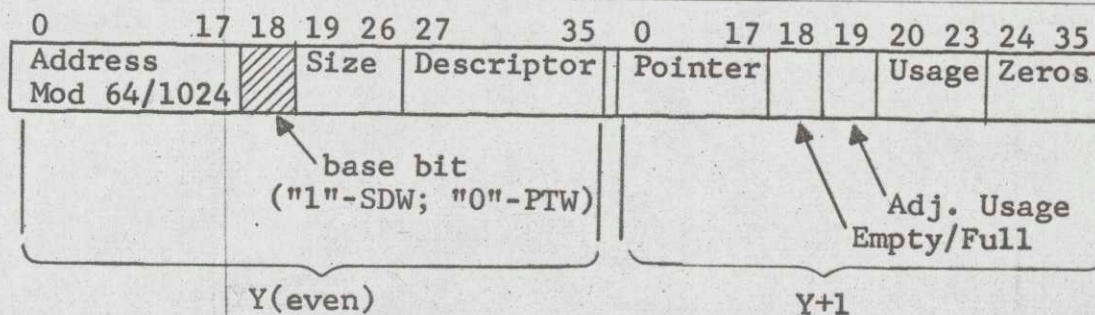
Spec. No. M50EB00107
 Cont. on Sh. A30 Sh. No. A29

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Data Movement-Store		
SAM	STORE ASSOCIATIVE MEMORY	557 ₈

Summary: $C(AM) \Rightarrow C(Y, \dots, Y+31)$ Where Y must be a 0 modulo 32 address.

Description: The contents of the Associative Memory (16 words) are stored in sequence as even-odd word pairs in double-word stores. The initial value is assigned by the hardware (that is, Associative Memory Register 0 stored in first word pair ... Associative Memory Register 15 stored in 16th word pair). If this instruction is attempted in Slave mode an Illegal Procedure fault will be generated. The format of the word pair stored in memory is as follows:



Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 29.87 - 33.33 μ sec (absolute/append)

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A31 Sh. No. A30

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Data Movement-Store
ZAM	STORE ASSOCIATIVE MEMORY ZERO	157 ₈

Summary: $C(AR) \Rightarrow C(Y, Y+1)$ when $C(AR)_{56-59} = 0$ and Y is an even location.

Description: This instruction stores the $C(AR)$ that has a current zero usage value, that is, $C(AR)_{56-59} = 0$, into an even-odd word pair; the format being the same as the SAM instruction. If this instruction is attempted in Slave mode an Illegal Procedure fault is generated.

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 2.84 - 6.30 μ sec (absolute/append)

Indicators Affected: None

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Spec. No. M50EB00107
Cont. on Sh. A32 Sh. No. A31

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Store

SBRn

STORE ADDRESS BASE REGISTER n (n=0,1,...,7)

54n₈

Summary: $C(ABRn) \Rightarrow C(Y)_{0-23}; 00...0 \Rightarrow C(Y)_{24-35}$

where n may designate an internal or external ABR.

Description:

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 2.19 μ sec

Indicators Affected: None

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Spec. M50EB00107
Cont. on Sh. A33 Sh. No. A32

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

STB	STORE BASES	Data Movement-Store
		254 ₈

Summary: $C(ABR_0, \dots, ABR_7) \Rightarrow C(Y, \dots, Y+7)_{0-23}; 00\dots 0 \Rightarrow C(Y, \dots, Y+7)_{24-35}$

where Y must be a 0 modulo 8 address, that is, Y_{15-17} starts at 000, and is increased by 001 for each successive location.

Description: The contents of the eight ABR's are stored in sequence in double word stores.

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 8.25 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A34 Sh. No. A33

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Data Movement-Store
SDBR	STORE DESCRIPTOR SEGMENT BASE REGISTER	154 ₈

Summary: $C(DSBR) \Rightarrow C(Y)_{0-28}; 00...0 \Rightarrow C(Y)_{29-35}$

Description: This instruction maybe executed in Master mode only or an Illegal Procedure fault is generated.

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 2.19 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A35 Sh. No. A34

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

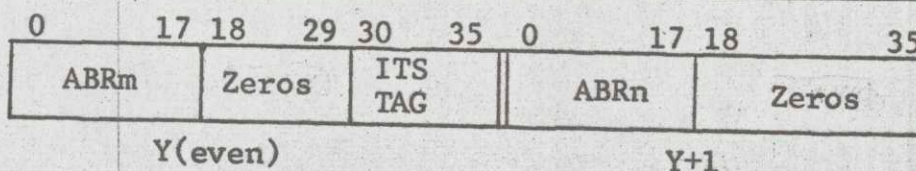
Data Movement-Store		
STPn	STORE PAIR n(n=0,1,...,7)	250-253 650-653 8

Summary:

(1) $C(ABR_m) \Rightarrow C(Y)_{0-17,00...0} \Rightarrow C(Y)_{18-29}$ ITS Tag (100011) $\Rightarrow C(Y)_{30-35}$ $C(ABR_n) \Rightarrow C(Y+1)_{0-17,00...0}$ $\Rightarrow C(Y+1)_{18-35}$	} if $C(ABR_n)_{21}=0$
(2) $C(ABR_m) \Rightarrow C(Y)_{0-17,00...0} \Rightarrow C(Y)_{18-29}$ ITS Tag (100011) $\Rightarrow C(Y)_{30-35}$ $00...0 \Rightarrow C(Y+1)_{0-35}$	

where n and m are the designated internal and linked external ABR's and Y is an even location.

Description: This instruction stores the contents of the internal ABR designated by the STPn instruction and the linked external ABR as an ITS-tagged even-odd word pair. If an external base is designated by the STPn instruction, that is, $C(ABR_n)_{21} = 1$, then an odd word of all zeros will be stored. The format of the word pair in memory is as follows:



Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 2.84 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh.A36 Sh. No. A35

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

STCD	STORE CONTROL DOUBLE	Data Movement-Store
		357 ₈

Summary: $C(PBR) \Rightarrow C(Y)_{0-17}, 00...0 \Rightarrow C(Y)_{18-29}, ITS \text{ Tag } (100011)$
 $\Rightarrow C(Y)_{30-35}; C(ICT)_C + 00...010 \Rightarrow C(Y+1)_{0-17}; C(IR) \Rightarrow$
 $C(Y+1)_{18-28}, 00...0 \Rightarrow C(Y+1)_{29-35}$ where Y is an even location.

Description: This instruction stores the $C(PBR, ICT_C + 00...010, IR)$ in an ITS-tagged even-odd word pair. The relationship between the bit positions of $C(Y+1)$ and the indicators are as follows:

Bit Position $C(Y+1)$	Indicators
18	Zero
19	Negative
20	Carry
21	Overflow
22	Exponent Overflow
23	Exponent Underflow
24	Overflow Mask
25	Tally Runout
26	Parity Error
27	Parity Mask
28	Absolute Mode

The format for the ITS-tagged word pair in memory is as follows:

0	17	18	29	30	35	0	17	18	28	29	35
PBR	Zeros			ITS Tag		ICT _C +00...010	IR		BLANK		
Y (even)						Y+1					

Modifications: All types except DU, DL, CI, SC, SCR. The state of the Tally Runout Indicator $C(Y+1)_{25}$ is not changed regardless of what address modification is performed on the STCD instruction for tally operations.

Timing: 2.84 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A37 Sh. No. A36

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

STA	STORE ACCUMULATOR	Data Movement-Store
		755 ₈

Summary: $C(A) \Rightarrow C(Y)$

Description:

Modifications: All except DU, DL.

Timing: 2.08 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A38 Sh. No. A37

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Store

STAC

STORE A CONDITIONAL

354₈

Summary: Test C(Y) Then:

- 1) if $C(Y) = 0$, $C(A) \Rightarrow C(Y)$ Zero indicator set ON
- 2) if $C(Y) \neq 0$, Zero indicator set OFF

Description: If the initial C(Y) is non-zero then C(Y) are not changed by this instruction.

Modifications: All types except DU, DL, CI, SC, SCR

Timing: 3.74 μ sec

Indicators Affected:

Zero	If initial $C(Y) = 0$, then ON; otherwise OFF
------	--

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Spec. No. M50EB00107

Cont. on Sh. A39 Sh. No. A38

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Store

STQ

STORE QUOTIENT REGISTER

756₈

Summary: $C(Q) \Rightarrow C(Y)$

Description:

Modifications: All except DU, DL.

Timing: 2.08 μ sec

Indicators Affected: None

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Spec. No.M50EB00107

Cont. on Sh. A40 Sh. No. A39

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Data Movement-Store
STAQ	STORE A-Q REGISTER	757 ₈

Summary: C(AQ) $\Rightarrow$ C(Y-pair)

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.61 μ sec

Indicators Affected: None

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Spec. No.M50EB00107

Cont. on Sh.A41 Sh. No. A40

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

STXn	STORE INDEX REGISTER n (n=0,1,...7)	Data Movement-Store 74n ₈
------	-------------------------------------	---

Summary: $C(X_n) \Rightarrow C(Y)_{0-17}$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.08 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A42 Sh. No. A41

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

SXLn	STORE INDEX REGISTER n IN LOWER (n=0,1,...,7)	Data Movement-Store 44n ₈
------	---	---

Summary: $C(Xn) \Rightarrow C(Y)_{18-35}$

Description:

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 2.08 μ sec

Indicators Affected: None

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Spec. No. M50EB00107
Cont. on Sh. A43 Sh. No. A42

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Data Movement-Store
SREG	STORE REGISTERS	753 ₈

Summary: $C(X_0, X_1, \dots, X_7, A, Q, E, TR) \Rightarrow C(Y, Y+1, \dots, Y+7)$
where Y must be an 0 modulo 8 address.

Description: The contents of the Index (X_0 - X_7), A-, Q-, E-, and TR- registers are stored in successive locations beginning at Y and ending at Y+7 in the following format:

$C(X_0) \Rightarrow C(Y)_{0-17}$	$C(X_6) \Rightarrow C(Y+3)_{0-17}$
$C(X_1) \Rightarrow C(Y)_{18-35}$	$C(X_7) \Rightarrow C(Y+3)_{18-35}$
$C(X_2) \Rightarrow C(Y+1)_{0-17}$	$C(A) \Rightarrow C(Y+4)_{0-35}$
$C(X_3) \Rightarrow C(Y+1)_{18-35}$	$C(Q) \Rightarrow C(Y+5)_{0-35}$
$C(X_4) \Rightarrow C(Y+2)_{0-17}$	$C(E) \Rightarrow C(Y+6)_{0-7};$
	$00\dots 0 \Rightarrow C(Y+6)_{8-35}$
$C(X_5) \Rightarrow C(Y+2)_{18-35}$	$C(TR) \Rightarrow C(Y+7)_{0-23},$
	$00\dots 0 \Rightarrow C(Y+7)_{24-36}$

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 8.59 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh.A44 Sh. No. A43

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

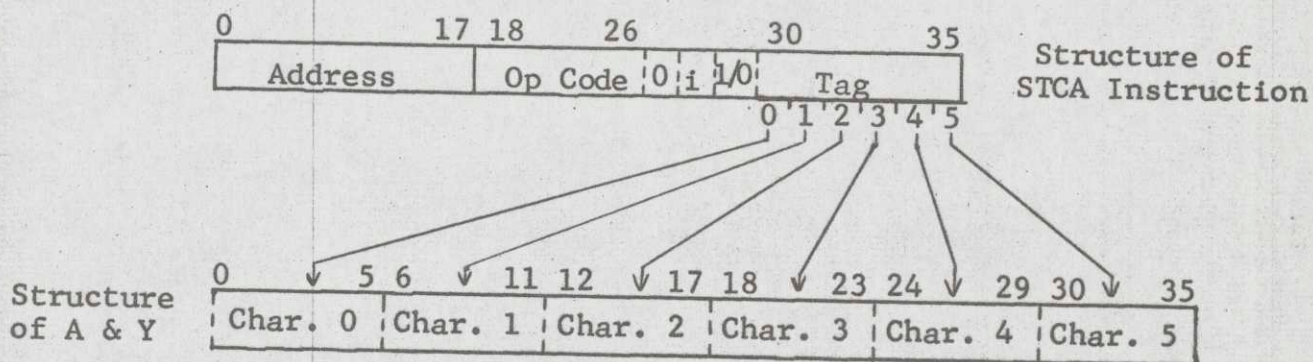
Data Movement-Store

STCA STORE CHARACTER of ACCUMULATOR (6 Bit)

751g

Summary: Specified 6-bit characters of C(A) $\Rightarrow$ corresponding characters of C(Y), the character positions affected being specified in the tag field of the STCA instruction.

Description: Binary ones in the tag field of this instruction specify the character positions of A and Y that are affected by this instruction as shown below:



Modifications: None can take place.

Timing: 2.08 μ sec

Indicators Affected: None

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Cont. on Sh..A45 Sh. No. A44

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

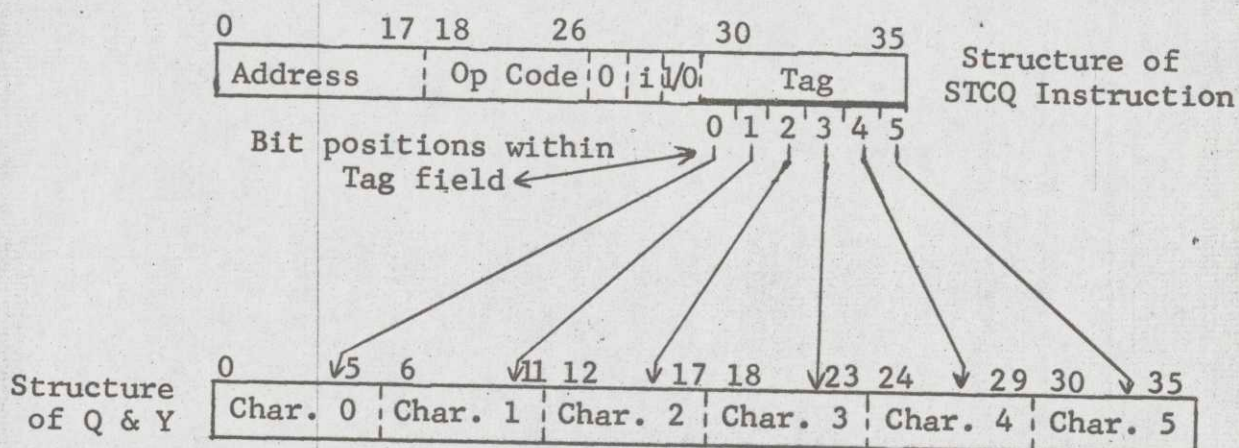
Data Movement-Store

STCQ STORE CHARACTER of QUOTIENT REGISTER (6 Bit)

752₈

Summary: Specified 6-bit characters of C(Q) $\Rightarrow$ corresponding characters of C(Y), the character positions affected being specified by the tag field of the STCQ instruction.

Description: Binary ones in the tag field of this instruction specify the character positions of Q and Y that are affected by this instruction as shown below:



Modifications: None can take place.

Timing: 2.08 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh.A46 Sh. No.A45

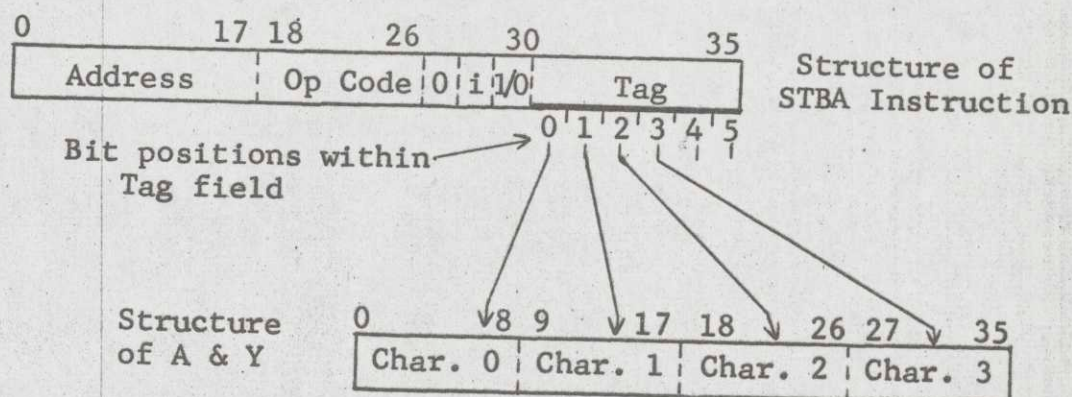
TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Data Movement-Store

STBA STORE CHARACTER of ACCUMULATOR (9 Bit) 551₈

Summary: Specified 9-bit characters of C(A) $\Rightarrow$ corresponding characters of C(Y), the character positions affected being specified by the tag field of the STBA instruction.

Description: Binary ones in the tag field of this instruction specify the character positions of A and Y that are affected by this instruction as shown below:



Modifications: No modifications can take place.

Timing: 2.08 μ sec

Indicators Affected: None

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Spec. No. M⁵⁰EB00107

Cont. on Sh. A7 Sh. No. A46

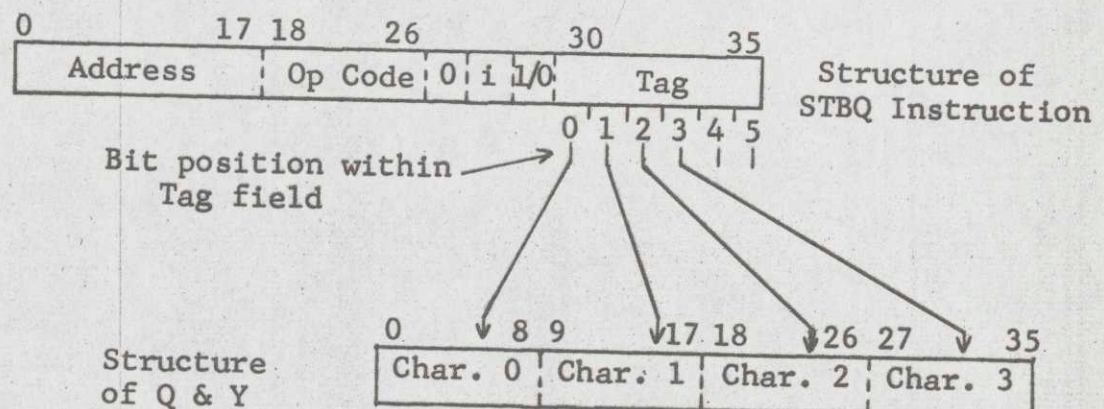
TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Store

STBQ STORE CHARACTER of QUOTIENT REGISTER (9 Bit) 552₈

Summary: Specified 9-bit characters of C(Q) $\Rightarrow$ corresponding characters of C(Y); the character positions affected being specified in the tag field of the STBQ instruction.

Description: Binary ones in the tag field of this instruction specify the character positions of Q and Y that are affected by this instruction as shown below:



Modifications: None can take place.

Timing: 2.08 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A48 Sh. No. A47

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Data Movement-Store
STI	STORE INDICATOR REGISTER	754 ₈

Summary: $C(IR) \Rightarrow C(Y)_{18-28}$

Description: The contents of the Indicator Register are stored in $C(Y)_{18-28}$ after modification, but the $C(Y)_{25}$ reflects the state of the Tally Runout indicator prior to modification. The relationship between $C(Y)_{18-28}$ and the indicators are as follows:

<u>Bit Position C(Y)</u>	<u>Indicator</u>
18	Zero
19	Negative
20	Carry
21	Overflow
22	Exponent Overflow
23	Exponent Underflow
24	Overflow Mask
25	Tally Runout
26	Parity Error
27	Parity Mask
28	Absolute Mode

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.47 μ sec

Indicators Affected: None

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Spec. No. M50EB00107
Cont. on Sh. A49 Sh. No. A48

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Store	
STT	STORE TIMER REGISTER 4548
<u>Summary:</u> $C(TR) \Rightarrow C(Y)_{0-23}; 00...0 \Rightarrow C(Y)_{24-35}$	
<u>Description:</u>	
<u>Modifications:</u> All except DU, DL, CI, SC, SCR.	
<u>Timing:</u> 2.41 μ sec	
<u>Indicators Affected:</u> None	

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Spec. No. M50EB00107
Cont. on Sh. A50 Sh. No. A49

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

SCU	STORE CONTROL UNIT	Data Movement-Store
		657 ₈

Summary: C(TBR) $\Rightarrow$ C(Y)₀₋₁₇, Appending Unit Status $\Rightarrow$ C(Y)₁₈₋₃₅
Computed Address $\Rightarrow$ C(Y+1)₀₋₁₇, Control Frame Status
 $\Rightarrow$ C(Y+1)₁₈₋₃₅, C(PBR) $\Rightarrow$ C(Y+2)₀₋₁₇, Fault Data $\Rightarrow$ C(Y+2)₁₈₋₃₅
C(ICTC) $\Rightarrow$ C(Y+3)₀₋₁₇, C(IR) $\Rightarrow$ C(Y+3)₁₈₋₂₈, Control Frame
Status $\Rightarrow$ C(Y+3)₃₀₋₃₅;
Even Instruction $\Rightarrow$ C(Y+4)₀₋₃₅
Odd Instruction $\Rightarrow$ C(Y+5)₀₋₃₅

Description: Detection of a fault or external interrupt condition will cause the taking of a snapshot of the CU status, storing it in temporary buffer registers, aborting the current sequence, and forcing an XED instruction pointing to an entry in a vector table corresponding to the particular fault or interrupt.

The SCU instruction is used specifically to store the buffered snapshot of the Control Unit immediately following interrupts or faults where eventual return to an exact point in the sequence is expected. Therefore, SCU must be used as the even instruction of an Execute Interrupt-or Fault Vector-pair.

If an attempt is made to issue SCU as a part of an instruction sequence, rather than in a vector following a "snapshot", the results described will not be obtained. The first double word is stored directly from the Data Out Register and contains whatever the last STORE+RAR left there. The second double word does store the PBR, ICT and IR. The third double word stores the instruction buffer registers and it may contain the next pair of instructions in the sequence, or any old pair of instructions. This type of usage may have some diagnostic value but is not generally recommended.

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Spec. No.M50EB00107

Cont. on Sh. A51 Sh. No. A50

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

If external interrupts are honored during address preparation cycles for SCU the current "snapshot" will be destroyed. Therefore, it is required that bit 28 of SCU is set to 1. SCU is a privileged instruction to be executed in Master mode only or an Illegal Procedure Fault will occur.

The effective address of an SCU instruction must be a 0 modulo eight number, that is, the three least significant bits are zero.

The execution of the SCU instruction involves the following actions:

- 1) $C(TBR) \Rightarrow C(Y)_{0-17}$

The contents of the Temporary Base Register whose snapshot now resides in the Data Out Register (bits 0-17) is stored in the upper half of Y.

- 2) Appending Unit Status $\Rightarrow C(Y)_{18-35}$

The appending unit registers and flags which constitute its status and whose snapshot now resides in the Data Out Register (bits 18-35) are stored in the lower half of Y as follows:

Bit Position	Name	
18-21	OSTR ₀₋₃	Odd Segment Tag Register & Use Flag
22-25	ESTR ₀₋₃	Even Segment Tag Register & Use Flag
26	ITS	ITS Tag
27	ITB	ITB Tag
28		Zero (Not Used)
29	PEO	Parity Error, Operand
30	ITR	Indirect Tally Not Equal to Tally Runout Indicator
31		Zero (Not Used)
32		Zero (Not Used)
33	DS PTW	Descriptor Segment PTW Fetch
34	SDW	Segment Descriptor Word Fetch
35	PTW	Page Table Word Fetch

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

3) Computed Address $\Rightarrow C(Y+1)_{0-17}$

The address, which had been generated during the address preparation cycle, and was snapshot in the Data Out Register (bits 36-53), is stored in the upper half of Y+1.

This may be the address of an operand, indirect word, or an instruction. Applicable registers (index, external base) are included.

4) Control Frame Status $\Rightarrow C(Y+1)_{18-35}$

The snapshot of the control frame registers and flags that constitute it's status and whose snapshot now resides in the Data Out Register (bits 54-71) is stored in the lower half of Y+1 as follows:

Bit Position	Name	Definition
18	PI	Instruction Fetch (1) Address Modifications (0)
19	PN	Indirect Address-Forced no address modification
20		Not Used
21	XDE	Execute Double Even
22	XDO	Execute Double Odd
23	IC	Even (0) or Odd (1) Instruction
24	MASF	Temporary Absolute Mode
25	EA	Operand (1) Indirect Fetch (0)
26	M/S	Master (1) Slave (0)
27	PA	Initial Address Preparation
28	PZ	Indirect Address Preparation (IR+RI)
29	PT	Indirect Address Preparation (IT)
30-35	CT ₀₋₅	Control Tag Register

5) $C(PBR) = C(Y+2)_{0+17}$

The Procedure Base Register is stored in the upper half of Y+2.

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Spec. No. M50EB00107

Cont. on Sh. A53 Sh. No. A52

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

6) Fault Data $\Rightarrow C(Y+2)_{18-35}$

Information on the fault is stored in the lower half of Y+2 as follows:

<u>Bit Position</u>	<u>Name</u>
18-20	Processor Number (000-111)
21	Illegal Procedure type a
22	Illegal Procedure type b
23	Illegal Procedure type c
24	Illegal Procedure type d
25	Illegal Procedure type e
26-30	Fault Code (00000-11111)
31-35	Zero (Not Used)

[See Section
2.9 on Faults]

7) $C(ICTC) \Rightarrow C(Y+3)_{0-17}$

The Instruction Counter is stored in the upper half of Y+3.

In the case of an interrupt during an operand, or an indirect word address preparation, the ICTC specifies the location of the active instruction. In the case of an interrupt prior to an instruction fetch, the ICTC specifies the address of the last successfully executed instruction.

It should be noted that in the case of a fault on an XEC'ed or XED'ed instruction, the ICTC points to the location of the original XEC or XED instruction, rather than the location of the faulting instruction.

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Spec. No. M50EB00107

Cont. on Sh. A54 Sh. No. A53

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

8) $C(IR) = C(Y+3)_{18-28}, 0 \Rightarrow C(Y+3)_{29}$

The contents of the Indicator Register will be stored in Y+3 as follows:

<u>Bit Position</u>	<u>Indicators</u>
18	Zero
19	Negative
20	Carry
21	Overflow
22	Exponent Overflow
23	Exponent Underflow
24	Overflow Mask
25	Tally Runout
26	Parity Error
27	Parity Mask
28	Absolute Mode

The $C(Y+3)_{25}$ will contain the State of the Tally Runout indicator prior to address modification of the instruction (for tally operations).

9) Control Frame Status $\Rightarrow C(Y+3)_{30-33}, 00 \Rightarrow C(Y+3)_{34,35}$

The status flags of the Control Frame will be stored in Y+3 as follows:

<u>Bit Position</u>	<u>Name</u>	<u>Definition</u>
30	RF	Initial Repeated Instruction
31	FT	Repeat
32	FL	Repeat Link
33	FD	Repeat Double

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Spec. No. M50EB00107

Cont. on Sh. A55 Sh. No. A54

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10) EVEN Instruction $\Rightarrow C(Y+4)_{0-35}$

11) ODD Instruction $\Rightarrow C(Y+5)_{0-35}$

The active pair of instructions, is stored in Y+4 and Y+5. If the interrupt occurred prior to an instruction fetch (PI cycle), then these instructions have already been executed. If the interrupt occurred during address preparation for an indirect word or an operand, then if IC = 0 the faulting instruction is the even one, or if IC = 1 the faulting instruction is the odd. The address field of the faulting instruction, $C(Y+4 \text{ or } 5)_{0-17}$, contains the address field of the instruction, or the last indirect word, or the last indirect word minus one or delta. The tag field of the faulting instruction, $C(Y+4 \text{ or } 5)_{30-35}$, contains the tag of the original instruction or the last indirect word.

Modifications: All types except DU, DL, CI, SC, SCR, F1, F2, F3.

Timing: 6.44 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A56 Sh. No. A55

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Store

STC1 STORE INSTRUCTION COUNTER plus 1 554₈

Summary: $C(ICTC) + 0...01 \Rightarrow C(Y)_{0-17}$

$C(IR) \Rightarrow (Y)_{18-28}; 00...0 \Rightarrow C(Y)_{29-35}$

Description: The contents of the Instruction Counter and the Indicator Register are stored in $C(Y)_{0-17}$ and $C(Y)_{18-28}$ respectively after modification. The $C(Y)_{25}$ reflects the state of the Tally Runout indicator prior to modification. The relationship between the $C(Y)_{18-28}$ and the indicators are as follows:

<u>Bit Position C(Y)</u>	<u>Indicators</u>
18	Zero
19	Negative
20	Carry
21	Overflow
22	Exponent Overflow
23	Exponent Underflow
24	Overflow Mask
25	Tally Runout
26	Parity Error
27	Parity Mask
28	Absolute Mode

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.47 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A57 Sh. No. A56

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Store

STC2

STORE INSTRUCTION COUNTER plus 2

750₈

Summary: $C(IC) + 0...010 \Rightarrow C(Y)_{0-17}$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.47 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A58 Sh. No. A57

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Store

STZ

STORE ZERO

450₈

Summary: 00...0 $\Rightarrow$ C(Y)

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.39 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A59 Sh. No. A58

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Shift

ARS

ACCUMULATOR RIGHT SHIFT

731₈

Summary: Shift C(A) right by Y_{11-17} positions; fill vacated C(A) with $C(A)_0$.

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.47 μ sec

Indicators Affected:

Zero	If $C(A) = 0$, then ON; otherwise OFF
Negative	If $C(A)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A60 Sh. No. A59

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		<u>Data Movement-Shift</u>
QRS	QUOTIENT REGISTER RIGHT SHIFT	732 ₈

Summary: Shift the $C(Q)$ right by Y_{11-17} positions; fill vacated $C(Q)$ with $C(Q)_0$.

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.47 μ sec

Indicators Affected:

Zero	If $C(Q) = 0$, then ON; otherwise OFF
Negative	If $C(Q)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A61 Sh. No. A60

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Shift

LRS

LONG RIGHT SHIFT

733₈

Summary: Shift the C(AQ) right by Y₁₁₋₁₇ positions; fill vacated C(AQ) with C(A)₀.

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.47 μ sec

Indicators Affected:

Zero	If C(AQ) = 0, then ON; otherwise OFF
Negative	If C(AQ) ₀ = 1, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A62 Sh. No. A61

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Shift

ALS

ACCUMULATOR LEFT SHIFT

735₈

Summary: Shift the C(A) left by Y₁₁₋₁₇ positions; fill vacated C(A) with zeros.

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.47 μ sec

Indicators Affected:

Zero	If C(A) = 0, then ON; otherwise OFF
Negative	If C(A) ₀ = 1, then ON; otherwise OFF
Overflow	If C(A) ₀ ever changes during the shift, then ON; otherwise OFF

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Spec. No. M50EB00107
Cont. on Sh.A63 Sh. No. A62

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Shift

QLS QUOTIENT REGISTER LEFT SHIFT 736₈

Summary: Shift the C(Q) left by Y₁₁₋₁₇ positions; fill vacated C(Q) with zeros.

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.47 μ sec

Indicators Affected:

Zero	If C(Q) = 0, then ON; otherwise OFF
Negative	If C(Q) ₀ = 1, then ON; otherwise OFF
Overflow	If C(Q) ₀ ever changes during the shift, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A64 Sh. No. A63

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Shift

LLS

LONG LEFT SHIFT

737₈

Summary: Shift the C(AQ) left by Y₁₁₋₁₇ positions; fill vacated C(AQ) with zeros.

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.47 μ sec

Indicators Affected:

Zero	If C(AQ) = 0, then ON; otherwise OFF
Negative	If C(AQ) ₀ = 1, then ON; otherwise OFF
Overflow	If C(AQ) ₀ ever changes during the shift, then ON; otherwise OFF

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Spec. No. M50EB00107
Cont. on Sh. A65 Sh. No. A64

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Data Movement-Shift
ARL	ACCUMULATOR RIGHT LOGICAL	771 ₈

Summary: Shift the C(A) right by Y₁₁₋₁₇ positions; fill vacated C(A) with zeros.

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.47 μ sec

Indicators Affected:

Zero	If $C(A) = 0$, then ON; otherwise OFF
Negative	If $C(A)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A66 Sh. No. A65

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Data Movement-Shift
QRL	QUOTIENT REGISTER RIGHT LOGICAL	772 ₈

Summary: Shift C(Q) right by Y₁₁₋₁₇ positions; fill vacated C(Q) with zeros.

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.47 μ sec

Indicators Affected:

Zero	If C(Q) = 0, then ON; otherwise OFF
Negative	If C(Q) ₀ = 1, then ON; otherwise OFF

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Spec. No. M50EB00107
Cont. on Sh. A67 Sh. No. A66

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

LRL	LONG RIGHT LOGICAL	Data Movement-Shift
		773 ₈

Summary: Shift C(AQ) right by Y₁₁₋₁₇ positions; fill vacated C(AQ) with zeros.

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.47 μ sec

Indicators Affected:

Zero	If C(AQ) = 0, then ON; otherwise OFF
Negative	If C(AQ) ₀ = 1, then ON; otherwise OFF

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Spec. No. M50EB00107
Cont. on Sh. A68 Sh. No. A67

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Data Movement-Shift
ALR	ACCUMULATOR LEFT ROTATE	775 ₈

Summary: Rotate the C(A) by Y₁₁₋₁₇ positions; enter each bit leaving A₀ into A₃₅.

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.47 μ sec

Indicators Affected:

Zero	If C(A) = 0, then ON; otherwise OFF
Negative	If C(A) ₀ = 1, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A69 Sh. No. A68

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Shift

QLR

QUOTIENT REGISTER LEFT ROTATE

776₈

Summary: Rotate the C(Q) by Y₁₁₋₁₇ positions; enter each bit leaving Q₀ into Q₃₅.

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.47 μ sec

Indicators Affected:

Zero	If $C(Q) = 0$, then ON; otherwise OFF
Negative	If $C(Q)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh.A70 Sh. No.A69

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Data Movement-Shift

LLR

LONG LEFT ROTATE

777₈

Summary: Rotate the C(AQ) left by Y_{11-17} positions; enter each bit leaving A_0 into Q_{35} .

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.47 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107
Cont. on Sh. A71 Sh. No. A70

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Addition

ADbn	ADD to ADDRESS BASE REGISTER n (n=0,1,.....,7)	050-053 150-153 ₈
------	--	---------------------------------

Summary: $C(Y)_{0-17} + C(ABRn)_{0-17} \Rightarrow C(ABRn)_{0-17}$

Description: This instruction may be executed in Master or Slave Mode. If attempted in Slave mode an Illegal Procedure Fault is generated unless $C(ABRn)_{22} = 0$. The ABR specified by the ADbn instruction may be an internal or external base ($C(ABRn)_{21} = 0$ or 1).

Modifications: All types except CI, SC, SCR.

Timing: 3.31 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A72 Sh. No. A71

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Addition

ADA

ADD to ACCUMULATOR

075₈

Summary: $C(A) + C(Y) \Rightarrow C(A)$

Description:

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(A) = 0$, then ON; otherwise OFF
Negative	If $C(A)_0 = 1$, then ON; otherwise OFF
Overflow	If range of A is exceeded, then ON
Carry	If a carry out of A_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A73 Sh. No. A72

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Addition

ADQ ADD to QUOTIENT REGISTER

076₈

Summary: $C(Q) + C(Y) \Rightarrow C(Q)$

Description:

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Q) = 0$, then ON; otherwise OFF
Negative	If $C(Q)_0 = 1$, then ON; otherwise OFF
Overflow	If range of Q is exceeded, then ON
Carry	If a carry out of Q_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A74 Sh. No. A73

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Addition

ADAA

ADD to A-Q REGISTER

077₈

Summary: $C(AQ) + C(Y\text{-pair}) \Rightarrow C(AQ)$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.87 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF
Overflow	If range of AQ exceeded, then ON
Carry	If carry out of AQ_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A75 Sh. No. A74

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Addition

ADXn ADD to INDEX REGISTER n (n=0,1,...,7) 06ng

Summary: $C(Xn) + C(Y)_{0-17} \Rightarrow C(Xn)$

Description:

Modifications: All except CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Xn) = 0$, then ON; otherwise OFF
Negative	If $C(Xn)_0 = 1$, then ON; otherwise OFF
Overflow	If range of Xn is exceeded; then ON
Carry	If a carry out of Xn_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107
Cont. on Sh. A76 Sh. No. A75

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Addition

ASA

ADD STORED to ACCUMULATOR

055₈

Summary: $C(A) + C(Y) \Rightarrow C(Y)$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 3.74 μ sec

Indicators Affected:

Zero	If $C(Y) = 0$, then ON; otherwise OFF
Negative	If $C(Y)_0 = 1$, then ON; otherwise OFF
Overflow	If range of Y is exceeded, then ON
Carry	If carry out of Y_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107
Cont. on Sh. A77 Sh. No. A76

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Addition

ASQ ADD STORED to QUOTIENT REGISTER 056₈

Summary: $C(Q) + C(Y) \Rightarrow C(Y)$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 3.74 μ sec

Indicators Affected:

Zero	If $C(Y) = 0$ then ON; otherwise OFF
Negative	If $C(Y)_0 = 1$, then ON; otherwise OFF
Overflow	If range of Y is exceeded, then ON
Carry	If a carry out of Y_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A78 Sh. No. A77

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Addition

ASXn ADD STORED to INDEX REGISTER n (n=0,1,...,7) 04n₈

Summary: $C(X_n) + C(Y)_{0-17} \Rightarrow C(Y)_{0-17}$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 3.73 μ sec

Indicators Affected:

Zero	If $C(Y)_{0-17} = 0$, then ON; otherwise OFF
Negative	If $C(Y)_0 = 1$, then ON; otherwise OFF
Overflow	If range of Y_{0-17} exceeded, then ON
Carry	If a carry out of Y_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107
Cont. on Sh. A79 Sh. No. A78

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Addition

ADLA ADD LOGICAL to ACCUMULATOR 035₈

Summary: $C(A) + C(Y) \Rightarrow C(A)$

Description: The contents of the Accumulator are added to the contents of the location specified by the absolute address Y. The Overflow indicator is not affected; otherwise, this instruction is identical to the ADA instruction.

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(A) = 0$, then ON; otherwise OFF
Negative	If $C(A)_0 = 1$, then ON; otherwise OFF
Overflow	Not affected
Carry	If a carry out of A_0 is generated then ON, otherwise OFF

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Spec. No. M50EB00107
Cont. on Sh. A80 Sh. No. A79

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Addition

ADLQ

ADD LOGICAL to QUOTIENT REGISTER

036₈

Summary: $C(Q) + C(Y) \Rightarrow C(Q)$

Description: The contents of the Quotient Register are added to the contents of the location specified by the absolute address Y. The Overflow indicator is not affected; otherwise, this instruction is identical to the ADQ instruction.

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Q) = 0$, then ON; otherwise OFF
Negative	If $C(Q)_0 = 1$, then ON; otherwise OFF
Overflow	Not affected
Carry	If a carry out of Q_0 is generated then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A81 Sh. No. A80

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Addition

ADLAQ

ADD LOGICAL to A-Q REGISTER

037₈

Summary: $C(AQ) + C(Y\text{-pair}) \Rightarrow C(AQ)$

Description: The contents of the combined Accumulator Quotient register is added to the contents of the location specified by the absolute address of the Y-pair. The Overflow indicator is not affected; otherwise, this instruction is identical to the ADAQ instruction.

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.87 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF
Overflow	Not affected
Carry	If carry out of AQ_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A82 Sh. No. A81

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Addition

ADLXn ADD LOGICAL to INDEX REGISTER n (n=0,1,...,7) 02n₈

Summary: $C(X_n) + C(Y)_{0-17} \Rightarrow C(X_n)$

Description: The contents of the Index Register specified are added to bits 0-17 of the location specified by the absolute address Y. The Overflow indicator is not affected; otherwise, this instruction is identical to the ADXn instruction.

Modifications: All except CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(X_n) = 0$, then ON; otherwise OFF
Negative	If $C(X_n)_0 = 1$, then ON; otherwise OFF
Overflow	Not Affected
Carry	If a carry out of X_{n0} is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A83 Sh. No. A82

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Addition

AWCA

ADD with CARRY to ACCUMULATOR

071₈

Summary: Carry Indicator ON: $C(A) + C(Y) + 0\dots01 \Rightarrow C(A)$
Carry Indicator OFF: $C(A) + C(Y) \Rightarrow C(A)$

Description: The contents of the location specified by the absolute address Y are added to the contents of the Accumulator. If the Carry indicator is ON, a "1" is added to the A₃₅ position of the Accumulator; otherwise this instruction is identical to the ADA instruction.

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(A) = 0$, then ON; otherwise OFF
Negative	If $C(A)_0 = 1$, then ON; otherwise OFF
Overflow	If range of A is exceeded, then ON
Carry	If a carry out of A ₀ is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A84 Sh. No. A83

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Addition

AWCQ ADD with CARRY to QUOTIENT REGISTER 072₈

Summary: Carry Indicator ON: $C(Q) + C(Y) + 0...01 \Rightarrow C(Q)$
 Carry Indicator OFF: $C(Q) + C(Y) \Rightarrow C(Q)$

Description: The contents of the location specified by the absolute address Y is added to the contents of the Quotient Register. If the Carry indicator is ON a "1" is added to the Q35 position of the Quotient Register; otherwise, this instruction is identical to the ADQ instruction.

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Q) = 0$, then ON; otherwise OFF
Negative	If $C(Q)_0 = 1$, then ON; otherwise OFF
Overflow	If range of Q is exceeded, then ON
Carry	If carry out of Q_0 is generated, then ON, otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A85 Sh. No. A84

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Addition

ADL

ADD LOW to A-Q REGISTER

033₈

Summary: $C(AQ) + C(Y)$ sign extended, $\Rightarrow C(AQ)$

Description: A 72-bit number is formed from $C(Y)$ by extending the sign of $C(Y)$ 36 bits to fill in the upper half of the 72-bit number; the lower 36 bits containing $C(Y)$. This number is added to the combined A-Q register effecting the addition of $C(Y)$ to the lower half of the combined A-Q register, with a possible carry out of the Q part being passed to the A part.

Modifications: All except CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF
Overflow	If range of AQ is exceeded, then ON
Carry	If a carry out of AQ_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A86 Sh. No. A85

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Addition

AOS

ADD ONE to STORAGE

054₈

Summary: $C(Y) + 0 \dots 01 \Rightarrow C(Y)$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 3.73 μ sec

Indicators Affected:

Zero	If $C(Y) = 0$, then ON; otherwise OFF
Negative	If $C(Y)_0 = 1$, then ON; otherwise OFF
Overflow	If range of Y is exceeded, then ON
Carry	If a carry out of Y_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A87 Sh. No. A86

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Subtraction

SBA

SUBTRACT from ACCUMULATOR

175₈

Summary: $C(A) - C(Y) \Rightarrow C(A)$

Description:

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(A) = 0$, then ON; otherwise OFF
Negative	If $C(A)_0 = 1$, then ON; otherwise OFF
Overflow	If range of A is exceeded, then ON
Carry	If a carry out of A_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A88 Sh. No. A87

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Subtraction

SBQ

SUBTRACT from QUOTIENT REGISTER

176₈

Summary: $C(Q) - C(Y) \Rightarrow C(Q)$

Description:

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Q) = 0$, then ON; otherwise OFF
Negative	If $C(Q)_0 = 1$, then ON; otherwise OFF
Overflow	If range of Q is exceeded, then ON
Carry	If a carry out of Q_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A89 Sh. No. A88

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Subtraction

SBAQ	SUBTRACT FROM A-Q REGISTER	177 ₈
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Summary: $C(AQ) - C(Y\text{-pair}) \Rightarrow C(AQ)$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.87 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF
Overflow	If range of AQ exceeded, then ON
Carry	If carry out of AQ_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A90 Sh. No. A89

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Subtraction

SBXn SUBTRACT from INDEX REGISTER n ($n=0,1,\dots,7$) 16ng

Summary: $C(Xn) - C(Y)_{0-17} \Rightarrow C(Xn)$

Description:

Modifications: All except CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Xn) = 0$, then ON; otherwise OFF
Negative	If $C(Xn)_0 = 1$, then ON; otherwise OFF
Overflow	If range of Xn is exceeded, then ON
Carry	If a carry out of Xn_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A91 Sh. No. A90

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Subtraction

SSA

SUBTRACT STORED from ACCUMULATOR

155₈

Summary: $C(A) - C(Y) \Rightarrow C(Y)$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 3.73 μ sec

Indicators Affected:

Zero	If $C(Y) = 0$, then ON; otherwise OFF
Negative	If $C(Y)_0 = 1$, then ON; otherwise OFF
Overflow	If range of Y is exceeded, then ON
Carry	If a carry out of Y_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A92 Sh. No. A91

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Subtraction

SSQ

SUBTRACT STORED from QUOTIENT REGISTER

156₈

Summary: $C(Q) - C(Y) \Rightarrow C(Y)$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 3.74 μ sec

Indicators Affected:

Zero	If $C(Y) = 0$, then ON; otherwise OFF
Negative	If $C(Y)_0 = 1$, then ON; otherwise OFF
Overflow	If range of Y is exceeded, then ON
Carry	If a carry out of Y_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A93 Sh. No. A92

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Subtraction

SSXn SUBTRACT STORED from INDEX REGISTER n ($n=0,1,\dots,7$) $14n_8$

Summary: $C(Xn) - C(Y)_{0-17} \Rightarrow C(Y)_{0-17}$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 3:74 μ sec

Indicators Affected:

Zero	If $C(Y)_{0-17} = 0$, then ON; otherwise OFF
Negative	If $C(Y)_0 = 1$, then ON; otherwise OFF
Overflow	If range of Y_{0-17} exceeded, then ON
Carry	If a carry out of Y_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh.A94 Sh. No.A93

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Subtraction

SBLA

SUBTRACT LOGICAL FROM ACCUMULATOR

135₈

Summary: $C(A) - C(Y) \Rightarrow C(A)$

Description: This instruction is identical to the SBA instruction except that the Overflow indicator is not affected by this instruction.

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(A) = 0$, then ON; otherwise OFF
Negative	If $C(A)_0 = 1$, then ON; otherwise OFF
Overflow	Not affected
Carry	If a carry out of A_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A95 Sh. No. A94

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Subtraction

SBLQ SUBTRACT LOGICAL FROM QUOTIENT REGISTER 136₈

Summary: $C(Q) - C(Y) \Rightarrow C(Q)$

Description: This instruction is identical to the SBQ instruction except that the Overflow indicator is not affected by this instruction.

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Q) = 0$, then ON; otherwise OFF
Negative	If $C(Q)_0 = 1$, then ON; otherwise OFF
Overflow	Not affected
Carry	If a carry out of Q_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A96 Sh. No. A95

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Subtraction

SBLAQ

SUBTRACT LOGICAL from A-Q REGISTER

137₈

Summary: $C(AQ) - C(Y\text{-pair}) \Rightarrow C(AQ)$

Description: This instruction is identical to the SBAQ instruction except the Overflow indicator is not affected by this instruction.

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.87 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF
Overflow	Not affected
Carry	If a carry out of AQ_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A97 Sh. No. A96

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic - Subtraction

SBLXn SUBTRACT LOGICAL from INDEX REGISTER n ($n=0,1,\dots,7$) $12n_8$

Summary: $C(Xn) - C(Y)_{0-17} \Rightarrow C(Xn)$

Description: This instruction is identical to the SBXn instruction except that the Overflow indicator is not affected by this instruction.

Modifications: All except CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Xn) = 0$, then ON; otherwise OFF
Negative	If $C(Xn)_0 = 1$, then ON; otherwise OFF
Overflow	Not affected
Carry	If a carry out of Xn_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A98 Sh. No. A97

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Subtraction

SWCA SUBTRACT with CARRY from ACCUMULATOR 171₈

Summary: Carry Indicator ON: $C(A) - C(Y) \Rightarrow C(A)$
OFF: $C(A) - C(Y) - 0...01 \Rightarrow C(A)$

Description: This instruction is used for multiple-word precision arithmetic and is identical to the SBA instruction, except that if the Carry indicator is OFF at the beginning of instruction execution, + 1 is subtracted from the least significant position of the Accumulator (A₃₅).

Expressed differently:

Carry Indicator ON: $C(A) + 1\text{'s complement of } C(Y) + 0...01 \Rightarrow C(A)$

OFF: $C(A) + 1\text{'s complement of } C(Y) \Rightarrow C(A)$

The binary 0...01 in the first expression represents the carry from the previous multiple-length subtraction; the C(Y) is being subtracted from C(A). In the second expression with no carry, + 1 is effectively being subtracted from $[C(A) - C(Y)]$

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(A) = 0$, then ON; otherwise OFF
Negative	If $C(A)_0 = 1$, then ON; otherwise OFF
Overflow	If the range of A is exceeded, then ON
Carry	If a carry out of A ₀ is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A99 Sh. No. A98

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Subtraction

SWCQ SUBTRACT with CARRY from QUOTIENT REGISTER 172₈

Summary: Carry Indicator ON: $C(Q) - C(Y) \Rightarrow C(Q)$
OFF: $C(Q) - C(Y) - 0...01 \Rightarrow C(Q)$

Description: This instruction is used for multiple-word precision arithmetic and is identical to the SBQ instruction, except that if the Carry indicator is OFF at the beginning of instruction execution, + 1 is subtracted from the least significant position of the Quotient Register (Q₃₅).

Expressed differently:

Carry Indicator ON: $C(Q) + 1\text{'s complement of } C(Y) + 0...01 \Rightarrow C(Q)$

OFF: $C(Q) + 1\text{'s complement of } C(Y) \Rightarrow C(Q)$

The binary 0...01 in the first expression represents the carry from the previous multiple-length subtraction; the C(Y) is being subtracted C(Q). In the second expression with no carry, + 1 effectively being subtracted from $[C(Q) - C(Y)]$.

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Q) = 0$, then ON; otherwise OFF
Negative	If $C(Q)_0 = 1$, then ON; otherwise OFF
Overflow	If range of Q is exceeded, then ON
Carry	If carry out of Q ₀ is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A100 Sh. No. A99

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Multiplication

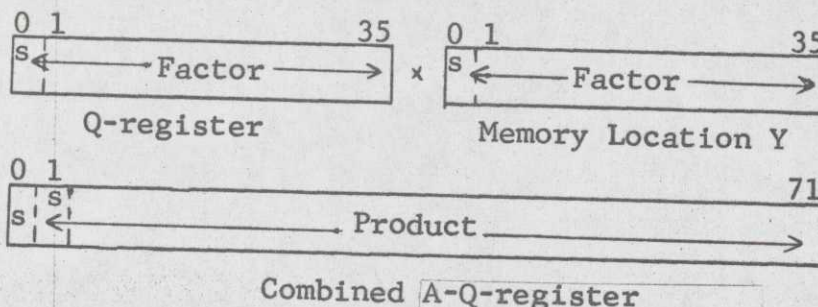
MPY

MULTIPLY INTEGER

4028

Summary: $C(Q) \times C(Y) \Rightarrow C(AQ)$ right justified

Description: Two 36-bit integer factors (including sign) are multiplied to form a 71-bit integer product (including sign) which is stored in the A-Q-register right adjusted. Bit position AQ_0 is filled with an "extended sign" bit. For $-2^{35} \times -2^{35} = +2^{70}$, AQ_1 is used to represent the product rather than as an extension of the sign. No overflow can occur.



Modifications: All except CI, SC, SCR.

Timing: 7.09 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107
 Cont. on Sh. A101 Sh. No. A100

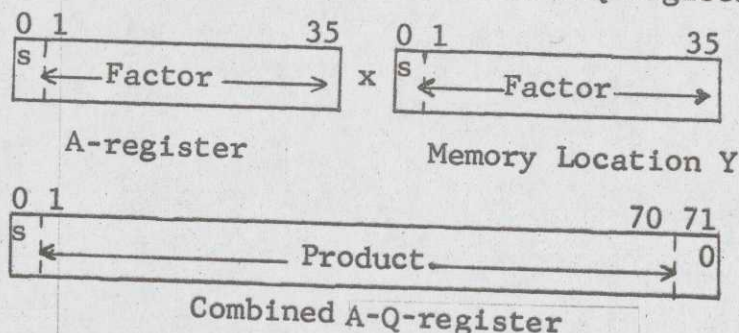
TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Multiplication

MPF MULTIPLY FRACTION 401₈

Summary: $C(A) \times C(Y) \Rightarrow C(AQ)$ left justified

Description: Two 36-bit fractional factors (including sign) are multiplied to form a 71-bit fractional product (including sign), which is stored left justified in the A-Q-register; bit position AQ₇₁ is filled with zero. Overflow can occur only in the case of A and Y containing all "1"s and the result exceeding the combined A-Q-register.



Modifications: All except CI, SC, SCR.

Timing: 7.09 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF
Overflow	If range of AQ is exceeded, then ON

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Spec. No. M50EB00107

Cont. on Sh.A102 Sh. No. A101

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Division

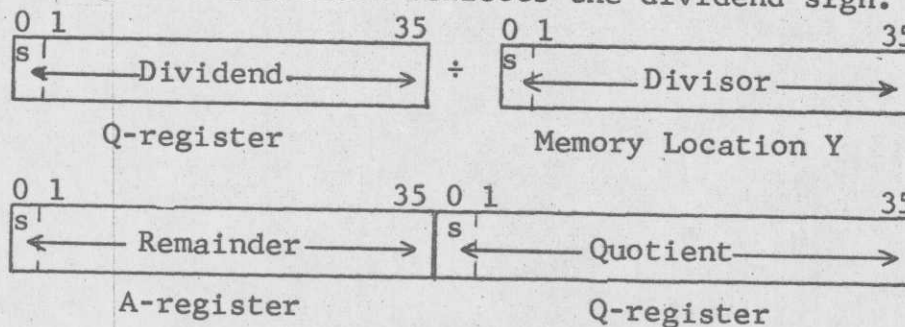
DIV

DIVIDE INTEGER

506₈

Summary: $C(Q) \div C(Y)$; integer quotient $\Rightarrow C(Q)$
 fractional remainder $\Rightarrow C(A)$

Description: A 36-bit integer dividend including sign, is divided by a 36-bit integer divisor including sign to form a 36-bit integer quotient including sign and a 36-bit fractional remainder including sign. The remainder sign is equal to the dividend sign unless the remainder is zero. If the dividend = -2^{35} and divisor = -1 , or if the divisor = 0, then the divisor itself does not take place a Divide-Check Fault Trap occurs and $C(Y)$ remains unchanged, $C(Q)$ contains the dividend magnitude in Absolute, and the Negative indicator reflects the dividend sign.



Modifications: All types

Timing: 14.12 μ sec

Indicators Affected:

	If division takes place:	If no division takes place:
Zero	If $C(Q) = 0$, then ON; otherwise OFF	If divisor = 0, then ON; otherwise OFF
Negative	If $C(Q)_0 = 1$, then ON; otherwise OFF	If dividend < 0 , then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A103 Sh. No. A102

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Division

DVF

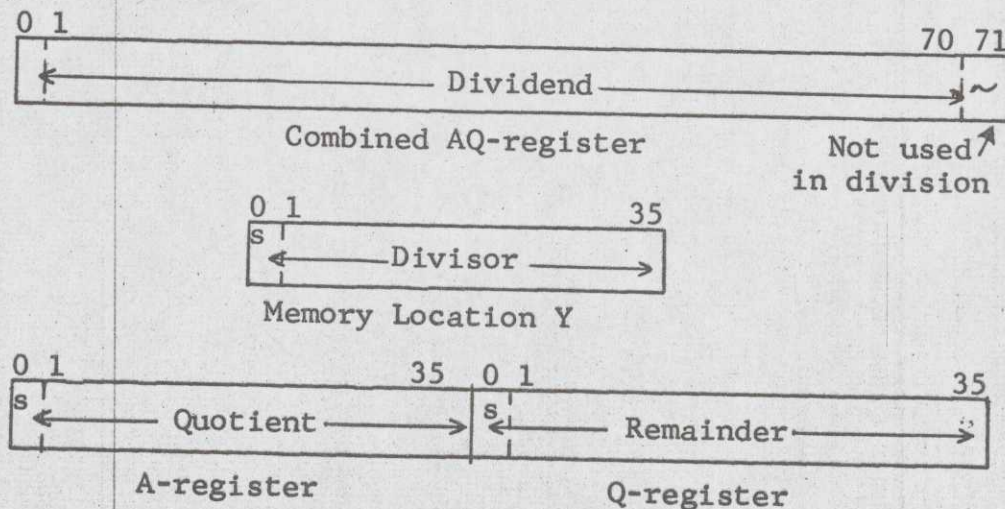
DIVIDE FRACTION

507₈

Summary: $C(AQ) \div C(Y)$; fractional quotient $\Rightarrow C(A)$
 remainder $\Rightarrow C(Q)$

Description: A 71-bit fractional dividend (including sign) is divided by a 36-bit fractional divisor (including sign) to form a 36-bit fractional quotient (including sign) and a 36-bit remainder (including sign), bit position 35 of the remainder corresponding to bit position 70 of the dividend. The remainder sign is equal to the dividend-sign unless the remainder is zero.

If the $|dividend| \geq |divisor|$ or if the divisor = 0, then the division itself does not take place, a Divide-Check Fault Trap occurs, the divisor $C(Y)$ remains unchanged, the $C(AQ)$ contains the dividend magnitude in absolute, and the Negative indicator reflects the dividend sign.



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Spec. No. M50EB001Q7

Cont. on Sh. A104 Sh. No. A103

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic-Division

DVF

DIVIDE FRACTION (cont.)

507₈

Modifications: All types

Timing: 14.12 μ sec

Indicators Affected:

	If division takes place:	If no division takes place:
Zero	If $C(A) = 0$, then ON; otherwise OFF	If divisor = 0, then ON; otherwise OFF
Negative	If $C(A)_0 = 1$, then ON; otherwise OFF	If dividend < 0 , then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A105 Sh. No. A104

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed Point-Arithmetic-Negate

NEG

NEGATE ACCUMULATOR

531₈

Summary: $-C(A) \Rightarrow C(A)$

Description: The number contained in the Accumulator is changed to its negative (if $\neq 0$) by forming the 2's complement of the string of 36-bits.

Modifications: Are without any effect on the operation.

Timing: 1.51 μ sec

Indicators Affected:

Zero	If $C(A) = 0$, then ON; otherwise OFF
Negative	If $C(A)_0 = 1$, then ON; otherwise OFF
Overflow	If range of A is exceeded, then ON

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Spec. No. M50EB00107

Cont. on Sh. A106 Sh. No. A105

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Fixed-Point Arithmetic - Negate

NEGL

NEGATE LONG

5338

Summary: $-C(AQ) = C(AQ)$

Description: The number contained in the combined A-Q-register is changed to its negative (if $\neq 0$) by forming the 2's complement of the string of the bits.

Modifications: Are without any effect on the operation.

Timing: 1.51 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF
Overflow	If range of AQ exceeded, then ON

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Spec. No. M50EB00107

Cont. on Sh.A107 Sh. No. A106

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Load

FLD	FLOATING LOAD	
		431 ₈

Summary: $C(Y)_{0-7} \Rightarrow C(E)$, $C(Y)_{8-35} \Rightarrow C(AQ)_{0=29; 00...0} \Rightarrow C(AQ)_{30-71}$

Description:

Modifications: All types except CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A108 Sh. No. A107

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Load

DFLD	DOUBLE-PRECISION FLOATING LOAD	4338
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Summary: $C(Y\text{-pair})_{0-7} \Rightarrow C(E)$, $C(Y\text{-pair})_{8-71} \Rightarrow C(AQ)_{0-63}$,
 $00\dots 0 \Rightarrow C(AQ)_{64-71}$

Description:

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 1.87 μsec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A109 Sh. No. A108

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Load

LDE

LOAD EXPONENT REGISTER

4118

Summary: $C(Y)_{0-7} \Rightarrow C(E)$

Description:

Modifications: All types except CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	Set OFF
Negative	Set OFF

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Spec. No. M50EB00107

Cont. on Sh. A110 Sh. No. A109

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

FST	FLOATING STORE	Floating-Point Arithmetic-Store
		4558

Summary: $C(E,A) \Rightarrow C(Y)$

Description: The contents of the combined EA-registers are truncated at A27 and stored in the location specified by Y as follows:

$C(E) \Rightarrow C(Y)_{0-7}$
 $C(A)_{0-27} \Rightarrow C(Y)_{8-35}$

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 2.08 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A111 Sh. No. A110

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Store

DFST

DOUBLE-PRECISION FLOATING STORE

457₈

Summary: $C(E,A,Q) \Rightarrow C(Y\text{-pair})$

Description: The contents of the combined EAQ-registers are truncated at Q63 and stored in the location specified by the Y-pair as follows:

$C(E) \Rightarrow C(Y\text{-pair})_{0-7}$
 $C(AQ)_{0-63} \Rightarrow C(Y\text{-pair})_{8-71}$

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 2.61 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A112 Sh. No. A111

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Store

STE

STORE EXPONENT REGISTER

456₈

Summary: $C(E) = C(Y)_{0-7}; 00\dots 0 \Rightarrow C(Y)_{8-17}$

Description:

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 2.08 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A113 Sh. No. A112

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Addition

FAD

FLOATING ADD

475₈

Summary: $C(EAQ) + C(Y)$ normalized $\Rightarrow C(EAQ)$

Description:

Modifications: All types except CI, SC, SCR.

Timing: 1.99 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF
Exp. Overflow	If exponent above +127, then ON
Exp. Underflow	If exponent below -128, then ON
Carry	If carry out of AQ_0 is generated, then ON, otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A114 Sh. No. A113

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Addition

UFA	UNNORMALIZED FLOATING ADD	435 ₈
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Summary: $C(EAQ) + C(Y)$ not normalized $\Rightarrow C(EAQ)$

Description:

Modifications: All types CI, SC, SCR.

Timing: 1.99 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF
Exp. Overflow	If exponent above +127, then ON
Exp. Underflow	If exponent below -128, then ON
Carry	If a carry out of AQ_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A115 Sh. No. A114

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Addition

DFAD DOUBLE-PRECISION FLOATING ADD 477₈

Summary: $C(EAQ) + C(Y\text{-pair}) \text{ normalized} \Rightarrow C(EAQ)$

Description:

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 2.10 μsec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF
Exp. Overflow	If exponent above +127, then ON
Exp. Underflow	If exponent below -128, then ON
Carry	If carry out of AQ_0 is generated then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A116 Sh. No. A115

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Addition

DUFA	DOUBLE-PRECISION UNNORMALIZED FLOATING ADD	437 ₈
------	--	------------------

Summary: $C(EAQ) + C(Y\text{-pair}) \text{ not normalized} \Rightarrow C(EAQ)$

Description:

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 2.10 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF
Exp. Overflow	If exponent above -127, then ON
Exp. Underflow	If exponent below -128, then ON
Carry	If carry out of AQ_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A117 Sh. No. A116

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Addition

ADE

ADD TO EXPONENT REGISTER

4158

Summary: $C(E) + C(Y)_{0-7} \Rightarrow C(E)$

Description:

Modifications: All types except CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	Set OFF
Negative	Set OFF
Exp. Overflow	If exponent above +127, then ON
Exp. Underflow	If exponent below -128, then ON

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Spec. No. M50EB00107

Cont. on Sh.A118 Sh. No.A117

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Subtraction

FSB

FLOATING SUBTRACT

575₈

Summary: $C(EAQ) - C(Y) \text{ normalized} \Rightarrow C(EAQ)$

Description:

Modifications: All types except CI, SC, SCR.

Timing: 2.54 μsec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF
Exp. Overflow	If exponent above +127, then ON
Exp. Underflow	If exponent below -128, then ON
Carry	If a carry out of AQ_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A119 Sh. No. A118

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Subtraction

UFS

UNNORMALIZED FLOATING SUBTRACT

535₈

Summary: $C(EAQ) - C(Y)$ not normalized $\Rightarrow C(EAQ)$

Description:

Modifications: All types except CI, SC, SCR.

Timing: 2.54 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF
Exp. Overflow	If exponent above +127, then ON
Exp. Underflow	If exponent below -128, then ON
Carry	If carry out of AQ_0 is generated, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A120 Sh. No. A119

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Subtraction

DFSB DOUBLE-PRECISION FLOATING SUBTRACT

577₈

Summary: C(EAQ) - C(Y-pair) normalized $\Rightarrow$ C(EAQ)

Description:

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 2.54 μ sec

Indicators Affected:

Zero	If C(AQ) = 0, then ON, otherwise OFF
Negative	If C(AQ) ₀ = 1, then ON; otherwise OFF
Exp. Overflow	If exponent above +127, then ON
Exp. Underflow	If exponent below -128, then ON
Carry	If a carry out of AQ ₀ is generated, then ON, otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A121 Sh. No. A120

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Subtraction

DUFS

DOUBLE-PRECISION UNNORMALIZED FLOATING SUBTRACT 537_8

Summary: $C(EAQ) - C(Y\text{-pair})$ not normalized $\Rightarrow C(EAQ)$

Description:

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 2.54 μsec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON, otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON, otherwise OFF
Exp. Overflow	If exponent above +127, then ON
Exp. Underflow	If exponent below -128, then ON
Carry	If carry out of AQ_0 is generated, then ON, otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A122 Sh. No. A121

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Multiplication

FMP

FLOATING MULTIPLY

461₈

Summary: $C(EAQ) \times C(Y)$ normalized $\Rightarrow C(EAQ)$

Description: Execution of this instruction is as follows:

- 1) $C(E) + C(Y)_{0-7} \Rightarrow C(E)$
- 2) $C(AQ) \times C(Y)_{8-35}$ results in a 98-bit product plus sign, the leading 71 bits plus sign of which $\Rightarrow C(AQ)$
- 3) $C(EAQ)$ normalized $\Rightarrow C(EAQ)$

Modifications: All types except CI, SC, SCR.

Timing: 6.04 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF
Exp. Overflow	If exponent above +127, then ON
Exp. Underflow	If exponent below -128, then ON

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Spec. No. M50EB00107

Cont. on Sh. A123 Sh. No. A122

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Multiplication

UFM UNNORMALIZED FLOATING MULTIPLY 421₈

Summary: $C(EAQ) \times C(Y)$ not normalized $\Rightarrow C(EAQ)$

Description: This multiplication is executed like the FMP instruction except that final normalization is performed only in the case of both factor mantissas being equal to -1.00...0.

Modifications: All types except CI, SC, SCR.

Timing: 5.80 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON, otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF
Exp. Overflow	If exponent above +127, then ON
Exp. Underflow	If exponent below -128, then ON

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Spec. No. M50EB00107
Cont. on Sh. A124 Sh. No. A123

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Multiplication

DFMP

DOUBLE-PRECISION FLOATING MULTIPLY

463g

Summary: $C(EAQ) \times C(Y\text{-pair}) \text{ normalized} \Rightarrow C(EAQ)$

Description: Execution of this instruction is as follows:

- 1) $C(E) + C(Y\text{-pair})_{0-7} \Rightarrow C(E)$
- 2) $C(AQ) \times C(Y\text{-pair})_{8-71}$ results in a 134-bit product plus sign; the leading 71 bits plus sign of which $\Rightarrow C(AQ)$
- 3) $C(EAQ) \text{ normalized} \Rightarrow C(EAQ)$

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 11.85 μsec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON, otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON, otherwise OFF
Exp. Overflow	If exponent above +127, then ON
Exp. Underflow	If exponent below -128, then ON

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Spec. No. M50EB00107
Cont. on Sh. A125 Sh. No.. A124

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Multiplication

DUFM DOUBLE-PRECISION UNNORMALIZED FLOATING MULTIPLY 423₈

Summary: C(EAQ) x C(Y-pair) not normalized $\Rightarrow$ C(EAQ)

Description: This multiplication is executed like the instruction DFMP except that final normalization is performed only in the case of both factor mantissas being equal to -1.00...0.

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 11.61 μ sec

Indicators Affected:

Zero	If C(AQ) = 0, then ON, otherwise OFF
Negative	If C(AQ) ₀ = 1, then ON, otherwise OFF
Exp. Overflow	If exponent above +127, then ON
Exp. Underflow	If exponent below -128, then ON

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Division

FDV

FLOATING DIVIDE

565₈

Summary: $C(EAQ) \div C(Y) \Rightarrow C(EA); 00...0 \Rightarrow C(Q)$

Description: This instruction is executed as follows:

- 1) If the mantissa of the divisor = 0, then the division itself does not take place, a Divide-Check Fault Trap occurs and all the registers remain unchanged.
- 2) If the mantissa of the divisor $\neq 0$, then the dividend mantissa, $C(AQ)$ is shifted right and the dividend exponent $C(E)$ increased accordingly until:

$$|C(AQ)_{0-27}| < |C(Y)_{8-35}|.$$

Then:

$$C(E) - C(Y)_{0-7} \Rightarrow C(E);$$

$$C(AQ) \div C(Y)_{8-35} \Rightarrow C(A);$$

$$00...0 \Rightarrow C(Q).$$

Modifications: All types except CI, SC, SCR.

Timing: 14.52 μ sec

Indicators Affected:

Zero	If division takes place:	If no division takes place:
	If $C(A) = 0$, then ON, otherwise OFF	If divisor mantissa = 0, then ON, otherwise OFF
Negative	If $C(A)_0 = 1$, then ON, otherwise OFF	If dividend < 0 , then ON, otherwise OFF
Exp. Overflow	If exponent above + 127, then ON	
Exp. Underflow	If exponent below -128, then ON	

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Spec. No. M50EB00107
 Cont. on Sh. A127 Sh. No. A126

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Division

FDI FLOATING DIVIDE INVERTED 525₈

Summary: $C(Y) \div C(EAQ) \Rightarrow C(EA); 00\dots0 \Rightarrow C(Q)$

Description: This instruction is executed as follows:

- 1) If the mantissa of the divisor = 0, then the division itself does not take place, a Divide-Check Fault Trap occurs, and all registers remain unchanged.
- 2) If the mantissa of the divisor $\neq 0$, then the dividend mantissa, $C(Y)_{8-35}$, is shifted right and the dividend exponent $C(Y)_{0-7}$ increased accordingly until:
 $|C(Y)_{8-35}| < |C(AQ)_{0-27}|$.

Then:

$C(Y)_{0-7} - C(E) \Rightarrow C(E);$
 $C(Y)_{8-35} \div C(AQ) \Rightarrow C(A);$
 $00\dots0 \Rightarrow C(Q).$

Modifications: All types except CI, SC, SCR.

Timing: 14.12 μ sec

Indicators Affected:

Zero	If division takes place:	If no division takes place:
	If $C(A) = 0$, then ON, otherwise OFF	If divisor mantissa = 0, then ON, otherwise OFF
Negative	If $C(A)_0 = 1$, then ON, otherwise OFF	If dividend < 0 , then ON, otherwise OFF
Exp. Overflow	If exponent above +127, then ON	
Exp. Underflow	If exponent below -128, then ON	

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Spec. No. M50EB00107

Cont. on Sh. A128 Sh. No. A127

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Division

DFDV

DOUBLE PRECISION FLOATING DIVIDE

567₈

Summary: $C(EAQ) \div C(Y\text{-pair}) \Rightarrow C(EAQ)$

Description: This instruction is executed as follows:

- 1) If the mantissa of the divisor = 0, then the division does not take place, a Divide-Check Fault Trap occurs, and all registers remain unchanged.
- 2) If mantissa of divisor $\neq 0$, then the dividend mantissa $C(AQ)$ is shifted right and the dividend exponent $C(E)$ increased accordingly until:
 $|C(AQ)_{0-63}| < |C(Y\text{-pair})_{8-71}|$.

Then:

$$\begin{aligned} C(E) - C(Y\text{-pair})_{0-7} &\Rightarrow C(E) ; \\ C(AQ) \div C(Y\text{-pair})_{8-71} &\Rightarrow C(AQ)_{0-63}; \\ 00...0 &\Rightarrow C(AQ)_{64-71} \end{aligned}$$

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 23.56 μ sec

Indicators Affected:

	If division takes place:	If no division takes place:
Zero	If $C(AQ) = 0$, then ON, otherwise OFF	If divisor mantissa = 0, then ON, otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON, otherwise OFF	If dividend < 0 , then ON, then ON, otherwise OFF
Exp. Overflow	If exponent above +127, then ON	
Exp. Underflow	If exponent below -128, then ON	

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Spec. No M50EB00107

Cont. on Sh. A129 Sh. No. A128

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Division

DFDI

DOUBLE-PRECISION FLOATING DIVIDE INVERTED

527₈

Summary: $C(Y\text{-pair}) \div C(EAQ) \Rightarrow C(EAQ)$

Description: This instruction is executed as follows:

- 1) If the mantissa of the divisor = 0, then the division does not take place, a Divide-Check Fault Trap occurs, and all registers remain unchanged.
- 2) If the mantissa of the divisor $\neq 0$, then the dividend mantissa $C(Y\text{-pair})_{8-71}$ is shifted right and the dividend exponent $C(Y\text{-pair})_{0-7}$ increased accordingly until:
 $|C(Y\text{-pair})_{8-71}| < |C(AQ)_{0-63}|.$

Then:

$C(Y\text{-pair})_{0-7} - C(E) \Rightarrow C(E);$
 $C(Y\text{-pair})_{8-71} \div C(AQ) \Rightarrow C(AQ)_{0-63};$
 $00...0 \Rightarrow C(AQ)_{64-71}.$

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 23.15 μsec

Indicators Affected:

	If division takes place:	If no division takes place:
Zero	If $C(AQ) = 0$, then ON, otherwise OFF	If divisor mantissa = 0, then ON, otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON otherwise	If dividend < 0 , then ON, otherwise OFF
Exp. Overflow	If exponent above +127, then ON	
Exp. Underflow	If exponent below -128, then ON	

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Spec. No. M50EB00107

Cont. on Sh. A130 Sh. No. A129

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Negate

FNEG

FLOATING NEGATE

513₈

Summary: $-C(AQ)$ normalized $\Rightarrow C(AQ)$

Description: This instruction changes the number in EAQ to its normalized negative (if $C(AQ) \neq 0$) by first forming the 2's complement of $C(AQ)$ and then normalizing $C(EAQ)$. Exponent overflow can occur even if originally the $C(AQ)$ were normalized when $C(AQ) = -1.00...0$ and $C(E) = +127$.

Modifications: Have no effect on the operation.

Timing: 1.47 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON, else OFF
Negative	If $C(AQ)_0 = 1$, then ON, else OFF
Exp. Overflow	If exponent above +127, then ON
Exp. Underflow	If exponent below -128, then ON

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Spec. No. M50EB00107

Cont. on Sh. A131 Sh. No. A130

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Negate

FNO

FLOATING NORMALIZE

573₈

Summary: C(EAQ) normalized $\Rightarrow$ C(EAQ)

Description: This instruction normalizes the number in EAQ and can be used to correct overflows that have occurred with fixed-point numbers. If the Overflow indicator is ON then the number in the EAQ is normalized one place to the right, the sign bit C(AQ)₀ is inverted in order to reconstitute the actual sign, and the Overflow indicator is set OFF.

Modifications: Have no effect on the operation.

Timing: 1.47 μ sec

Indicators Affected:

Zero	If C(AQ) = 0, then ON, else OFF
Negative	If C(AQ) ₀ = 1, then ON, else OFF
Exp. Overflow	If exponent above +127, then ON
Exp. Underflow	If exponent below -128, then ON
Overflow	Set OFF

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Spec. No. M50EB00107

Cont. on Sh. A132 Sh. No. A131

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Compare

FCMP

FLOATING COMPARE

515₈

Summary: Algebraic comparison $C[(E)(AQ_{0-27})]:: C(Y)$

Description: Instruction execution is as follows: the $C(E)::C(Y)_{0-7}$, the number with the lowest exponent (E or Y_{0-7}) is selected and its mantissa is shifted right as many places as the difference of exponents. The mantissas are then compared and the status of the indicators are changed as indicated under Indicators Affected.

Modifications: All types except CI, SC, SCR.

Timing: 1.79 μ sec

Indicators Affected:

Zero	Negative	Relation
0	0	$C[(E)(AQ_{0-27})] > C(Y)$
1	0	$C[(E)(AQ_{0-27})] = C(Y)$
0	1	$C[(E)(AQ_{0-27})] < C(Y)$

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Spec. No. M50EB00107

Cont. on Sh. A133 Sh. No. A132

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Compare

FCMG

FLOATING COMPARE MAGNITUDE

425₈

Summary: Algebraic comparison $|C[(E)(AQ_{0-27})]| :: |C(Y)|$

Description: Instruction execution is as follows: the $C(E)::C(Y)_{0-7}$, the number with the lowest exponent (E or Y_{0-7}) is selected, and its mantissa shifted right as many places as the difference of exponents. The absolute value of the mantissas are then compared and the status of the indicators changed as indicated under Indicators Affected.

Modifications: All types except CI, SC, SCR.

Timing: 1.79 μ sec

Indicators Affected:

Zero	Negative	Relation
0	0	$ C[(E)(AQ_{0-27})] > C(Y) $
1	0	$ C[(E)(AQ_{0-27})] = C(Y) $
0	1	$ C[(E)(AQ_{0-27})] < C(Y) $

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Cont. on Sh. A134 Sh. No. A133

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

	Floating Point Arithmetic-Compare	
DFCMP	DOUBLE-PRECISION FLOATING COMPARE	5178

Summary: Algebraic comparison $C[(E)(AQ_{0-63})]::C(Y\text{-pair})$

Description: Instruction execution is as follows: the $C(E)::C(Y)_{0-7}$ the number with the lowest exponent (E or Y_{0-7}) is selected, and its mantissa shifted right as many places as the difference of exponents. The mantissas are then compared and the status of the indicators changed as indicated under Indicators Affected.

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 1.87 μ sec

Indicators Affected:

Zero	Negative	Relation
0	0	$C[(E)(AQ_{0-63})] > C(Y\text{-pair})$
1	0	$C[(E)(AQ_{0-63})] = C(Y\text{-pair})$
0	1	$C[(E)(AQ_{0-63})] < C(Y\text{-pair})$

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Spec. No. M50EB00107

Cont. on Sh. A135 Sh. No. A134

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Compare

DFCMG DOUBLE-PRECISION FLOATING COMPARE MAGNITUDE 427₈

Summary: Algebraic comparison $|C[(E)(AQ_{0-63})]| :: |C(Y\text{-pair})|$

Description: Instruction execution is as follows: the $C(E)::C(Y)_{0-7}$, the number with the lowest exponent (E or Y_{0-7}) is selected, and its mantissa shifted right as many places as the difference of exponents. The absolute value of the mantissas are then compared and the status of the indicators changed as indicated under Indicators Affected.

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 1.87μsec

Indicators Affected:

Zero	Negative	Relation
0	0	$ C[(E)(AQ_{0-63})] > C(Y\text{-pair}) $
1	0	$ C[(E)(AQ_{0-63})] = C(Y\text{-pair}) $
0	1	$ C[(E)(AQ_{0-63})] < C(Y\text{-pair}) $

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Spec. No. M50EB00107

Cont. on Sh. A136 Sh. No. A135

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Floating-Point Arithmetic-Compare

FSZN FLOATING SET ZERO AND NEGATIVE INDICATORS 430₈
 FROM MEMORY

Summary: Test the number C(Y), set indicators accordingly.

Description:

Modifications: All types except CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	Negative	Relation
0	0	mantissa $C(Y)_{8-35} > 0$
1	0	mantissa $C(Y)_{8-35} = 0$
0	1	mantissa $C(Y)_{8-35} < 0$

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Spec. No. M50EB00107
Cont. on Sh. A137 Sh. No. A136

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operations-AND

ANA

AND to ACCUMULATOR

375₈

Summary: $C(A)_i \text{ AND } C(Y)_i \Rightarrow C(A)_i$ for all $i=0,1,\dots,35$

Description:

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(A) = 0$, then ON; otherwise OFF
Negative	If $C(A)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A138 Sh. No. A137

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operations-AND

ANQ AND to QUOTIENT REGISTER 3768

Summary: $C(Q)_i \text{ AND } C(Y)_i \Rightarrow C(Q)_i$ for all $i=0,1,\dots,35$

Description:

Modifications: All types

Timing: 1.67 μsec

Indicators Affected:

Zero	If $C(Q) = 0$, then ON; otherwise OFF
Negative	If $C(Q)_0 = 1$, then ON; otherwise OFF

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Spec. No. M5CEB00107

Cont. on Sh. A139 Sh. No. A138

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation-AND

AN AQ AND to A-Q REGISTER 377₈

Summary: $C(AQ)_i \text{ AND } C(Y\text{-pair})_i \Rightarrow C(AQ)_i$ for all $i=0,1,\dots,71$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.87 μ sec

Indicators Affected:

Zero	If $C(AQ)_0 = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh.A140 Sh. No.A139

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation-AND

ANXn	AND to INDEX REGISTER n (n=0,1,...,7)	36n
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Summary: $C(Xn)_i \text{ AND } C(Y)_i \Rightarrow C(Xn)_i \text{ for } i=0,1,...,17$

Description:

Modifications: All except CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Xn) = 0$, then ON, otherwise OFF
Negative	If $C(Xn)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A141 Sh. No. A140

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation-AND

ANSA

AND to STORAGE ACCUMULATOR

355₈

Summary: $C(A)_i \text{ AND } C(Y)_i \Rightarrow C(Y)_i$ for all $i=0,1,\dots,35$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 3.73 μsec

Indicators Affected:

Zero	If $C(Y) = 0$, then ON; otherwise OFF
Negative	If $C(Y)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A142 Sh. No. A141

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation-AND

ANSQ AND to STORAGE QUOTIENT REGISTER 3568

Summary: $C(Q)_i \text{ AND } C(Y)_i \Rightarrow C(Y)_i$ for all $i=0,1,\dots,35$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 3.73 μ sec

Indicators Affected:

Zero	If $C(Y) = 0$, then ON; otherwise OFF
Negative	If $C(Y)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A143 Sh. No. A142

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation-AND

ANSXn AND to STORAGE INDEX REGISTER n (n=0,1,...,7) 34ng

Summary: $C(Xn)_i \text{ AND } C(Y)_i \Rightarrow C(Y)_i$ for all $i=0,1,...,17$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 3.73 μ sec

Indicators Affected:

Zero	If $C(Y) = 0$, then ON; otherwise OFF
Negative	If $C(Y)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A144 Sh. No. A143

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation-OR

ORA

OR to ACCUMULATOR

2758

Summary: $C(A)_i \text{ OR } C(Y)_i \Rightarrow C(A)_i$ for all $i=0,1,\dots,35$

Description:

Modifications: All types

Timing: 1.67 μsec

Indicators Affected:

Zero	If $C(A) = 0$, then ON; otherwise OFF
Negative	If $C(A)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh.A145 Sh. No. A144

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation-OR

ORQ	OR to QUOTIENT REGISTER	276 ₈
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Summary: $C(Q)_i \text{ OR } C(Y)_i \Rightarrow C(Q)_i$ for all $i=0,1,\dots,35$

Description:

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Q) = 0$, then ON; otherwise OFF
Negative	If $C(Q)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A146 Sh. No. A145

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation-OR

ORAQ

OR to A-Q REGISTER

277₈

Summary: $C(AQ)_i \text{ OR } C(Y\text{-pair})_i \Rightarrow C(AQ)_i$ for all $i=0,1,\dots,71$

Description:

Modifications: All except DU,DL,CI,SC.

Timing: 1.87 μsec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A147 Sh. No. A146

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation-OR

ORXn	OR to INDEX REGISTER n (n=0,1,...,7)	26ng
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Summary: $C(Xn)_i \text{ OR } C(Y)_i \Rightarrow C(Xn)_i$ for all $i=0,1,...,17$

Description:

Modifications: All except CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Xn) = 0$, then ON; otherwise OFF
Negative	If $C(Xn)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A148 Sh. No. A147

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation-OR

ORSA

OR to STORAGE ACCUMULATOR

255₈

Summary: $C(A)_i \text{ OR } C(Y)_i \Rightarrow C(Y)_i$ for all $i=0,1,\dots,35$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 3.73 μ sec

Indicators Affected:

Zero	If $C(Y) = 0$, then ON; otherwise OFF
Negative	If $C(Y)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A149 Sh. No. A148

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation-OR

ORSQ	OR to STORAGE QUOTIENT REGISTER	256 ₈
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Summary: $C(Q)_i \text{ OR } C(Y)_i \Rightarrow C(Y)_i$ for all $i=0,1,\dots,35$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 3.73 μsec

Indicators Affected:

Zero	If $C(Y) = 0$, then ON; otherwise OFF
Negative	If $C(Y)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A150 Sh. No. A149

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation-OR

ORSXn OR to STORAGE INDEX REGISTER n (n=0,1,...,7) 24ng

Summary: $C(Xn)_i \text{ OR } C(Y)_i \Rightarrow C(Y)_i$ for all $i=0,1,...,17$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 3.73 μ sec

Indicators Affected:

Zero	If $C(Y) = 0$, then ON; otherwise OFF
Negative	If $C(Y)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A151 Sh. No. A150

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation-Exclusive OR

ERA	EXCLUSIVE OR to ACCUMULATOR	6758
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Summary: $C(A)_i \neq C(Y)_i \Rightarrow C(A)_i$ for $i=0,1,\dots,35$

Description:

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(A) = 0$, then ON; otherwise OFF
Negative	If $C(A)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A152, Sh. No. A151

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation-Exclusive OR

ERQ	EXCLUSIVE OR to QUOTIENT REGISTER	676 ₈
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Summary: $C(Q)_i \neq C(Y)_i \Rightarrow C(Q)_i$ for $i=0,1,\dots,35$

Description:

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Q) = 0$, then ON; otherwise OFF
Negative	If $C(Q)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A153 Sh. No. A152

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation-Exclusive OR

ERAQ EXCLUSIVE OR to A-Q REGISTER

677₈

Summary: $C(AQ)_i \neq C(Y\text{-pair})_i \Rightarrow C(AQ)_i$ for all $i=0,1,\dots,71$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.87 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A154 Sh. No. A153

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation=Exclusive OR

ERXn EXCLUSIVE OR to INDEX REGISTER $n(n=0,1,\dots,7)$ 66ng

Summary: $C(Xn)_i \neq C(Y)_i \Rightarrow C(Xn)_i$ for $i=0,1,\dots,17$

Description:

Modifications: All except CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $C(Xn) = 0$, then ON; otherwise OFF
Negative	If $C(Xn)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A155 Sh. No. A154

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation-Exclusive OR

ERSA

EXCLUSIVE OR to STORAGE ACCUMULATOR

655₈

Summary: $C(A)_i \neq C(Y)_i \Rightarrow C(Y)_i$ for $i=0,1,\dots,35$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 3.73 μ sec

Indicators Affected:

Zero	If $C(Y) = 0$, then ON; otherwise OFF
Negative	If $C(Y)_0 = 1$, then ON; otherwise OFF

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Cont. on Sh. A156 Sh. No. A155

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation=Exclusive OR

ERSQ EXCLUSIVE OR to STORAGE QUOTIENT REGISTER 6568

Summary: $C(Q)_i \neq C(Y)_i \Rightarrow C(Y)_i$ for $i=0,1,\dots,35$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 3.73 μ sec

Indicators Affected:

Zero	If $C(Y) = 0$, then ON, otherwise OFF
Negative	If $C(Y)_0 = 1$, then ON, otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A157 Sh. No. A156

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Boolean Operation-Exclusive OR

ERSXn EXCLUSIVE OR to STORAGE INDEX REGISTER n ($n=0,1,\dots,7$) $64n_8$

Summary: $C(Xn)_i \neq C(Y)_i \Rightarrow C(Y)_i$ for $i=0,1,\dots,17$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 3.73 μ sec

Indicators Affected:

Zero	If $C(Y) = 0$, then ON; otherwise OFF
Negative	If $C(Y)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A158 Sh. No. A157

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Comparison-Compare		
CMPA	COMPARE WITH ACCUMULATOR	115 ₈

Summary: Comparison $C(A)::C(Y)$

Description: The contents of the Accumulator are compared with the contents of location specified by Y; the result is the status of the various indicators as shown below.

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	Negative	Carry	Algebraic Comparison	
			Relation	Sign
0	0	0	$C(A) > C(Y)$	$C(A)_0 = 0, C(Y)_0 = 1$
0	0	1	$C(A) > C(Y)$	} $C(A)_0 = C(Y)_0$
1	0	1	$C(A) = C(Y)$	
0	1	0	$C(A) < C(Y)$	
0	1	1	$C(A) < C(Y)$	$C(A)_0 = 1, C(Y)_0 = 0$

Zero	Carry	Logic Comparison
		Relation
0	0	$C(A) < C(Y)$
1	1	$C(A) = C(Y)$
0	1	$C(A) > C(Y)$

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Spec. No. M50EB00107

Cont. on Sh. A159 Sh. No. A158

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Comparison-Compare

CMPQ

COMPARE WITH QUOTIENT REGISTER

1168

Summary: Comparison $C(Q)::C(Y)$

Description: The contents of the Quotient Register are compared with the contents of the location specified by Y; the result is the status of the various indicators as shown below.

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	Negative	Carry	<u>Algebraic Comparison</u>	
			Relation	Sign
0	0	0	$C(Q) > C(Y)$	$C(Q)_0 = 0, C(Y)_0 = 1$
0	0	1	$C(Q) > C(Y)$	} $C(Q)_0 = C(Y)_0$
1	0	1	$C(Q) = C(Y)$	
0	1	0	$C(Q) < C(Y)$	
0	1	1	$C(Q) < C(Y)$	$C(Q)_0 = 1, C(Y)_0 = 0$

Zero	Carry	<u>Logic Comparison</u>
		Relation
0	0	$C(Q) < C(Y)$
1	1	$C(Q) = C(Y)$
0	1	$C(Q) > C(Y)$

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Spec. No. M50EB00107

Cont. on Sh. A160 Sh. No. A159

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Comparison-Compare		
CMPAQ	COMPARE WITH A-Q REGISTER	1178

Summary: Comparison $C(AQ)::C(Y\text{-pair})$

Description: The contents of the combined A-Q register are compared with the contents of the location specified by the Y-pair; the result is the status of the indicators as shown below:

Modifications: All types

Timing: 1.87 μsec

Indicators Affected:

Zero	Negative	Carry	<u>Algebraic Comparison</u>	
			Relation	Sign
0	0	0	$C(AQ) > C(Y\text{-pair})$	$C(AQ)_0 = 0, C(Y\text{-pair})_0 = 1$
0	0	1	$C(AQ) > C(Y\text{-pair})$	} $C(AQ)_0 = C(Y\text{-pair})_0$
1	0	1	$C(AQ) = C(Y\text{-pair})$	
0	1	0	$C(AQ) < C(Y\text{-pair})$	
0	1	1	$C(AQ) < C(Y\text{-pair})$	$C(AQ)_0 = 1, C(Y\text{-pair})_0 = 0$

Zero	Carry	<u>Logic Comparison</u>
		Relation
0	0	$C(AQ) < C(Y\text{-pair})$
1	1	$C(AQ) = C(Y\text{-pair})$
0	1	$C(AQ) > C(Y\text{-pair})$

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Spec. No. M50EB00107

Cont. on Sh. A161 Sh. No. A160

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Comparison-Compare		
CMPXn	COMPARE WITH INDEX REGISTER n (n=0,1,...,7)	10n ₈

Summary: Comparison $C(X_n) :: C(Y)_{0-17}$

Description:

Modifications: All types except CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	Negative	Carry	<u>Algebraic Comparison</u>	
			Relation	Sign
0	0	0	$C(X_n) > C(Y)_{0-17}$	$C(X_n)_0 = 0, C(Y)_0 = 1$
0	0	1	$C(X_n) > C(Y)_{0-17}$	} $C(X_n)_0 = C(Y)_0$
1	0	1	$C(X_n) = C(Y)_{0-17}$	
0	1	0	$C(X_n) < C(Y)_{0-17}$	
0	1	1	$C(X_n) < C(Y)_{0-17}$	$C(X_n)_0 = 1, C(Y)_0 = 0$

Zero	Carry	<u>Logic Comparison</u>
		Relation
0	0	$C(X_n) < C(Y)_{0-17}$
1	1	$C(X_n) = C(Y)_{0-17}$
0	1	$C(X_n) > C(Y)_{0-17}$

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Spec. No. M50EB00107

Cont. on Sh. A162 Sh. No. A161

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Comparison-Compare		
CWL	COMPARE WITH LIMITS	111 ₈

Summary: Algebraic comparison of $C(Y)$ with the closed interval $[C(A); C(Q)]$ and also with the number $C(Q)$.

Description:

Modifications: All types

Timing: 1.68 μ sec

Indicators Affected:

Zero	If $C(Y)$ is contained in the closed interval $[C(A); C(Q)]$ that is, either $C(A) \leq C(Y) \leq C(Q)$ or $C(A) \geq C(Y) \geq C(Q)$ then ON; otherwise OFF
------	---

Zero	Negative	Relation between $C(Q)$ and $C(Y)$	Signs of $C(Q)$ and $C(Y)$
0	0	$C(Q) > C(Y)$	$C(Q)_0 = 0, C(Y)_0 = 1$
0	1	$C(Q) \geq C(Y)$	$C(Q)_0 = C(Y)_0$
1	0	$C(Q) < C(Y)$	
1	1	$C(Q) < C(Y)$	$C(Q)_0 = 1, C(Y)_0 = 0$

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Spec. No. M50EB00107

Cont. on Sh. A163 Sh. No. A162

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Comparison-Compare

CMG

COMPARE MAGNITUDE

405₈

Summary: Algebraic comparison $|C(A)| :: |C(Y)|$

Description: The absolute value of the contents of the Accumulator is compared with the absolute value of the location specified by Y; the result is the status of the indicators as shown below.

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	Negative	Relation
0	0	$ C(A) > C(Y) $
1	0	$ C(A) = C(Y) $
0	1	$ C(A) < C(Y) $

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Spec. No. M50EB00107

Cont. on Sh. A164 Sh. No. A163

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Comparison-Compare

SZN SET ZERO and NEGATIVE INDICATORS from MEMORY 234₈

Summary: Test the C(Y)

Description: The number contained in the address specified by Y is tested and the result is the status of the indicators as shown below.

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	Negative	Relation
0	0	number C(Y) > 0
1	0	number C(Y) = 0
0	1	number C(Y) < 0

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Spec. No. M50EB00107
 Cont. on Sh.A165 Sh. No. A164

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Comparison-Compare

CMK COMPARE MASKED 211₈

Summary: $Z_i = \overline{C(Q)}_i$ AND $[C(A)_i \neq C(Y)_i]$ for all $i=0,1,\dots,35$

Description: This instruction compares the corresponding bit positions of A and Y that are not masked by a "1" in the corresponding bit positions of the Q-register. The indicators are affected in the following manner:

Zero indicator set ON if: for all $i = 0,1,\dots,35$

Q_i	A_i	Z_i
1	-	0
0	$\equiv Y_i$	0

otherwise OFF

Negative indicator set ON if:

Q_0	A_0	Z_0
0	$\neq Y_0$	1

otherwise OFF

Modifications: All types

Timing: 1.68 μ sec

Indicators Affected:

Zero	if $Z=0$, then ON, otherwise OFF
Negative	if $Z_0 = 1$, then ON, otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A166 Sh. No. A165

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Comparison-Comparative AND

CANA

COMPARATIVE AND WITH ACCUMULATOR

315₈

Summary: $Z_i = C(A)_i$ AND $C(Y)_i$ for all $i=0,1,\dots,35$

Description:

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $Z = 0$, then ON; otherwise OFF
Negative	If $Z_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A167 Sh. No. A166

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Comparison-Comparative AND

CANQ COMPARATIVE AND WITH QUOTIENT REGISTER 3168

Summary: $Z_i = C(Q)_i$ AND $C(Y)_i$ for all $i=0,1,\dots,35$

Description:

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $Z = 0$, then ON; otherwise OFF
Negative	If $Z_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A168 Sh. No. A167

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Comparison-Comparative AND		
CANAQ	COMPARATIVE AND WITH A-Q REGISTER	317 ₈

Summary: $Z_i = C(AQ)_i \text{ AND } C(Y\text{-pair})_i$ for all $i=0,1,\dots,71$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.87 μsec

Indicators Affected:

Zero	If $Z = 0$, then ON, otherwise OFF
Negative	If $Z_0 = 1$, then ON, otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A169 Sh. No. A168

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Comparison=Comparative AND

CANXn COMPARATIVE AND WITH INDEX REGISTER $n(n=0,1,\dots,7)$ 30ng

Summary: $Z_i = C(Xn)_i$ AND $C(Y)_i$ for all $i=0,1,\dots,17$

Description:

Modifications: All except CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $Z = 0$, then ON; otherwise OFF
Negative	If $Z_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A170 Sh. No. A169

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Comparison-Comparative NOT

CNAA

COMPARATIVE NOT WITH ACCUMULATOR

215₈

Summary: $Z_i = C(A)_i \text{ AND } \overline{C(Y)}_i$ for all $i=0,1,\dots,35$

Description:

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $Z = 0$, then ON; otherwise OFF
Negative	If $Z_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh.A171 Sh. No. A170

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Comparison-Comparative NOT

CNAQ

COMPARATIVE NOT WITH QUOTIENT REGISTER

216₈

Summary: $Z_i = C(Q)_i$ AND $\overline{C(Y)_i}$ for all $i=0,1,\dots,35$

Description:

Modifications: All types

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $Z = 0$, then ON; otherwise OFF
Negative	If $Z_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A172 Sh. No. A171

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Comparison-Comparative NOT

CNAAQ

COMPARATIVE NOT WITH A-Q REGISTER

217₈

Summary: $Z_i = C(AQ)_i$ AND $\overline{C(Y\text{-pair})_i}$ for all $i=0,1,\dots,71$

Description:

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.87 μ sec

Indicators Affected:

Zero	If $Z = 0$, then ON; otherwise OFF
Negative	If $Z_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A173 Sh. No. A172

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Comparison-Comparative NOT

CNAXn COMPARATIVE NOT WITH INDEX REGISTER $n(n=0,1,\dots,7)$ $20n_8$

Summary: $Z_i = C(Xn)_i$ AND $\overline{C(Y)_i}$ for all $i=0,1,\dots,17$

Description:

Modifications: All CI, SC, SCR.

Timing: 1.67 μ sec

Indicators Affected:

Zero	If $Z = 0$, then ON; otherwise OFF
Negative	If $Z_0 = 0$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A174 Sh. No. A173

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Control-Transfer
TRA	TRANSFER UNCONDITIONALLY	710 ₈

Summary: EA $\Rightarrow$ C(ICTC), C(TBR) $\Rightarrow$ C(PBR)

Description: The new Effective Address replaces the C(ICTC), and the new Pointer in TBR formed during the Appending process for the transfer address replaces C(PBR). Pointers in TBR may come from the following sources:

- C(PBR) when bit 29 of instruction word = 0
- C(ABR_m) when bit 29 of instruction word = 1 (m is an external ABR)
- C(ABR_m) when designated by an ITB modifier in the indirect word (m is an external ABR)
- C(TBR) when brought in as a result of an ITS modifier in the indirect word

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.0 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A175 Sh. No. A174

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Control-Transfer

TSBn	TRANSFER AND SET BASE n (n=0,1,...,7)	270-273 670-673 ₈
------	---------------------------------------	---------------------------------

Summary: $C(ICTC) + 00 \dots 01 \Rightarrow C(ABRn)_{0-17}$; $C(PBR) \Rightarrow C(ABRm)_{0-17}$;
 $EA \Rightarrow C(ICTC)$; $P \Rightarrow C(PBR)$

where n and m are the designated internal and the linked external ABR's respectively.

Description: If the ABR specified by the TSBn instruction is external, that is, $C(ABRn)_{21} = 1$; then $C(ICTC) + 00 \dots 01 \Rightarrow C(ABRn)_{0-17}$ does not take place. The Pointer formed during the Appending process for the transfer address replaces C(PBR). Pointers in TBR may come from the following sources:

- C(PBR) when bit 29 of instruction word = 0
- C(ABRm) when bit 29 of instruction word = 1
- C(ABRm) when designated by an ITB modifier in the indirect word (m is an external ABR)
- C(TBR) when brought in as a result of an ITS modifier in the indirect word

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Spec. No. M50EB00107

Cont. on Sh. A176 Sh. No. A175

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

This instruction may be executed in Master or Slave mode. If attempted in Slave mode an Illegal Procedure fault will be generated unless $C(ABRn, m)_{22} = 0$. The ABR's will be effected in the following manner:

- If $C(ABRn)_{22} = 1$, the fault is generated and $ABRn, m$ are not changed.
- If $C(ABRn)_{22} = 0$ and $C(ABRm)_{22} = 1$; then $ABRn$ is loaded, $ABRm$ is not loaded, and the fault is generated for $ABRm$.

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 2.0 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A177 Sh. No. A176

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Control-Transfer

TSX_n TRANSFER AND SET INDEX REGISTER n ($n=0,1,\dots,7$) 70_n

Summary: $C(ICTC) + 0\dots 01 \Rightarrow C(X_n) EA \Rightarrow C(ICTC), C(TBR) \Rightarrow C(PBR)$

Description: The new Effective Address replaces the $C(ICTC)$, and the new Pointer in TBR formed during the Appending process for the transfer address replaces $C(PBR)$. Pointers in TBR may come from the following sources:

- $C(PBR)$ when bit 29 of instruction word = 0
- $C(ABR_m)$ when bit 29 of instruction word = 1 (m is an external ABR)
- $C(ABR_m)$ when designated by an ITB modifier in the indirect word (m is an external ABR)
- $C(TBR)$ when brought in as a result of an ITS modifier in the indirect word

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.0 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A178 Sh. No. A177

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Control-Transfer
TSS	TRANSFER AND SET SLAVE	715 ₈

Summary: EA $\Rightarrow$ C(ICTC), C(TBR) $\Rightarrow$ C(PBR), Reset Absolute indicator

Description: The new Effective Address replaces the C(ICTC), and the new Pointer in TBR formed during the Appending process for the transfer address replaces C(PBR). Pointers in TBR may come from the following sources:

- C(PBR) when bit 29 of instruction word = 0
- C(ABRm) when bit 29 of instruction word = 1 (m is an external ABR)
- C(ABRm) when designated by an ITBmodifier in the indirect word (m is an external ABR)
- C(TBR) when brought in as a result of an ITS modifier in the indirect word

If this instruction is attempted in Slave mode a 635/645 compatibility fault will occur. When this instruction is executed in Master mode, the Absolute indicator is reset as the last thing prior to the fetch of the new (transferred) instruction unless bit 29 of TSS is on, or ITB or ITS indirection is specified.

It is recommended that TSS not be used to get out of Absolute mode, since if bit 29 = "1" or ITS or ITB indirection is not used, then the transfer is done in Absolute.

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.0 μ sec

Indicators Affected:

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Spec. No. M50EB00107
Cont. on Sh. A179 Sh. No. A178

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Control-Transfer
RET	RETURN	630 ₈

Summary: $C(Y)_{0-17} \Rightarrow C(ICTC)$; $C(Y)_{18-28} \Rightarrow C(IR)$; $C(Y)_{29-35}$ are not used

Description: The contents of the location specified by Y replace the contents of the Instruction Counter and Indicator Register. A possible change in status of the Absolute mode indicator takes place as the last part of the instruction execution. The Tally Runout indicator reflects the state of $C(Y)_{25}$ prior to address modification and is unaffected by any subsequent modification performed on the RET instruction. The relationship between $C(Y)_{18-28}$ and the indicators are as follows:

<u>Bit Position C(Y)</u>	<u>Indicator</u>
18	Zero
19	Negative
20	Carry
21	Overflow
22	Exponent Overflow
23	Exponent Underflow
24	Overflow Mask
25	Tally Runout
26	Parity Error
27	Parity Mask
28	Absolute Mode

Modifications: All except DU, DL, CI, SC, SCR:

Timing: 4.0 μ sec

Indicators Affected:

Absolute Mode	If corresponding bit in C(Y) is 1, and Processor is in Procedure-Master mode, then ON; otherwise OFF.
All other indicators	If corresponding bit in C(Y) is 1, then ON; otherwise OFF.

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Spec. No. M50EB00107

Cont. on Sh.A180 Sh. No.A179

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Control-Transfer
RTCD	RETURN DOUBLE	610 ₈

Summary: $C(Y)_{0-17} \Rightarrow C(PBR)$; $C(Y)_{18-35}$ is ignored
 $C(Y+1)_{0-17} \Rightarrow C(ICTC)$; $C(Y+1)_{18-28} \Rightarrow C(IR)$

Description: This instruction restores the ICTC, IR and PBR from the even-odd pair specified by Y, Y+1. The relationship between the indicators and the $C(Y+1)_{18-28}$ is the same as the RET instruction.

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 3.7 μ sec

Indicators Affected: The indicators status reflect the contents of $Y+1_{18-28}$, as previously listed for the RET instruction.

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Spec. No. M50EB00107
 Cont. on Sh.A181 Sh. No.A180

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

		Control-Transfer
RCU	RESTORE CONTROL UNIT	613 ₈

Summary: C(Y)₀₋₁₇ ⇒ C(TBR), C(Y)₁₈₋₃₅ ⇒ Appending Unit Status;
 C(Y+1)₁₈₋₃₅ ⇒ Control Frame Status;
 C(Y+2)₀₋₁₇ ⇒ C(PBR)
 C(Y+3)₀₋₁₇ ⇒ C(ICTC), C(Y+3)₁₈₋₂₈ ⇒ C(IR), C(Y+3)₃₀₋₃₅ ⇒
 Control Frame Status
 C(Y+4) ⇒ Even Instruction
 C(Y+5) ⇒ Odd Instruction

Description: This instruction can only be used in Master mode.
 If attempted in Slave mode an Illegal Procedure
 Fault will occur.

The execution of the RCU instruction involves the
 following actions.

- 1) C(Y)₀₋₁₇ ⇒ C(TBR)
 The contents of the upper half of Y replaces the
 contents of the Temporary Base Register.
- 2) C(Y)₁₈₋₃₅ ⇒ Appending Unit Status
 The contents of the lower half of Y will affect the
 Appending Unit registers and flags as follows:

Bit Position	Action
18-21	Replaces the contents of OSTR ₀₋₃
22-25	Replaces the contents of ESTR ₀₋₃
26	If a "1" set ITS Flag, if a "0" reset ITS Flag.
27	If a "1" set ITB Flag, if a "0" reset ITB Flag.
28-29	No effect
30	If a "1" set HTAL, if a "0" reset HTAL
31-35	No effect

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

		Control-Transfer
RCU	RESTORE CONTROL UNIT cont.	613 8

3) $C(Y+1)_{18-35} \Rightarrow$ Control Frame Status

The contents of the lower half of Y+1 will affect the control frame registers and flags as follows:

Bit Position	Action
18	If a "1" set PI, if a "0" reset PI
19	If a "1" set PN, if a "0" reset PN
20	No effect
21	If a "1" set XDE, if a "0" reset XDE
22	If a "1" set XDO, if a "0" reset XDO
23	If a "1" set IC, if a "0" reset IC
24	If a "1" set MASF, if a "0" reset MASF
25	If a "1" set EA, if a "0" reset EA
26	If a "1" set MS, if a "0" reset MS
27	If a "1" set PA, if a "0" reset PA
28	If a "1" set PZ, if a "0" reset PZ
29	If a "1" set PT, if a "0" reset PT
30-35	Replaces the contents of CT ₀₋₅

4) $C(Y+2)_{0-17} \Rightarrow C(PBR)$

The contents of the upper half of Y+2 replaces the contents of the Procedure Base Register.

5) $C(Y+3)_{0-17} \Rightarrow C(ICTC)$

The contents of the upper half of Y+3 replaces the contents of the Instruction Counter.

6) $C(Y+3)_{18-28} \Rightarrow C(IR)$

The contents of bits 18-28 of Y+3 affect the Indicator Register as follows:

Bit Position	Action
18	If a "1" set Zero, if a "0" reset Zero
19	If a "1" set Negative, if a "0" reset Negative
20	If a "1" set Carry, if a "0" reset Carry
21	If a "1" set Overflow, if a "0" reset Overflow
22	If a "1" set Exponent Overflow, if a "0" reset Exponent Overflow

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Spec. No. M50EB00107

Cont. on Sh. A183 Sh. No. A182

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

RCU	RESTORE CONTROL UNIT cont.	Control-Transfer
		613

- | | |
|----|--|
| 23 | If a "1" set Exponent Underflow, if a "0" reset Exponent Underflow |
| 24 | If a "1" set Overflow Mask, if a "0" reset Overflow Mask |
| 25 | If a "1" set Tally Runout, if a "0" reset Tally Runout |
| 26 | If a "1" set Parity Error, if a "0" reset Parity Error |
| 27 | If a "1" set Parity Mask, if a "0" reset Parity Mask |
| 28 | If a "1" set Absolute Mode, if a "0" reset Absolute Mode |

- 7) $C(Y+3)_{30-35} \Rightarrow$ Control Frame Status
 The contents of Y+3, bits 30-35, affect the Control Frame status as follows:

Bit Position	Action
30	If a "1" set RF, if a "0" reset RF
31	If a "1" set FT, if a "0" reset FT
32	If a "1" set FL, if a "0" FL
33	If a "1" set FD, if a "0" reset FD
34	No effect
35	No effect

- 8) $C(Y+4)_{0-35} \Rightarrow$ Even Instruction
 The contents of Y+4 replace the contents of the Even Instruction Register.
- 9) $C(Y+5)_{0-35} \Rightarrow$ Odd Instruction
 The contents of Y+5 replace the contents of the Odd Instruction Register.

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Spec. No. M50EB00107

Cont. on Sh.A184 Sh. No.A183

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Control-Transfer
RCU	RESTORE CONTROL UNIT cont.	613

Modifications: All types except DU, DL, CI, SC, SCR, F1, F2, F3;
though F1, F2, F3 are recognized by the hardware
but defeat the purpose of the RCU.

Timing: 4.6 μ sec

Indicators Affected: The RCU instruction of itself does not affect
the indicators, however, the contents of Y+3
bits 0-28 will be placed in the Indicator
Register.

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Spec. No. M50EB00107

Cont. on Sh. A185 Sh. No. A184

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Control-Conditional Transfer

TZE

TRANSFER ON ZERO

600₈

Summary: If Zero indicator ON, then $EA \Rightarrow C(ICTC)$, $C(TBR) \Rightarrow C(PBR)$

Description: The new Effective Address replaces the $C(ICTC)$, and the new Pointer in TBR formed during the Appending process for the transfer address replaces $C(PBR)$. Pointers in TBR may come from the following sources:

- $C(PBR)$ when bit 29 of instruction word = 0
- $C(ABR_m)$ when bit 29 of instruction word = 1 (m is an external ABR)
- $C(ABR_m)$ when designated by an ITB modifier in the indirect word (m is an external ABR)
- $C(TBR)$ when brought in as a result of an ITS modifier in the indirect word

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.0 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A186 Sh. No. A185

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Control-Condition Transfer

TNZ

TRANSFER ON NOT ZERO

601₈

Summary: If Zero indicator OFF, then $EA \Rightarrow C(ICTC)$, $C(TBR) \Rightarrow C(PBR)$

Description: The new Effective Address replaces the $C(ICTC)$, and the new Pointer in TBR formed during the Appending process for the transfer address replaces $C(PBR)$.
Pointers in TBR may come from the following sources:

- $C(PBR)$ when bit 29 of instruction word = 0
- $C(ABR_m)$ when bit 29 of instruction word = 1 (m is an external ABR)
- $C(ABR_m)$ when designated by an ITB modifier in the indirect word (m is an external ABR)
- $C(TBR)$ when brought in as a result of an ITS modifier in the indirect word

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.0 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A187 Sh. No. A186

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Control-Conditional Transfer

TMI

TRANSFER ON MINUS

604₈

Summary: If Negative indicator ON, then $EA \Rightarrow C(ICTC)$, $C(TBR) \Rightarrow C(PBR)$

Description: The new Effective Address replaces the $C(ICTC)$, and the new Pointer in TBR formed during the Appending process for the transfer address replaces $C(PBR)$. Pointers in TBR may come from the following sources:

- $C(PBR)$ when bit 29 of instruction word = 0
- $C(ABR_m)$ when bit 29 of instruction word = 1
(m is an external ABR)
- $C(ABR_m)$ when designated by an ITB modifier in the instruction word (m is an external ABR)
- $C(TBR)$ when brought in as a result of an ITS modifier in the instruction word

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.0 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A188 Sh. No. A187

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Control-Conditional Transfer
TPL	TRANSFER ON PLUS	605 ₈

Summary: If Negative indicator OFF, then $EA \Rightarrow C(ICTC)$, $C(TBR) \Rightarrow C(PBR)$

Description: The new Effective Address replaces the $C(ICTC)$, and the new Pointer in TBR formed during the Appending process for the transfer address replaces $C(PBR)$. Pointers in TBR may come from the following sources:

- $C(PBR)$ when bit 29 of instruction word = 0
- $C(ABR_m)$ when bit 29 of instruction word = 1 (m is an external ABR)
- $C(ABR_m)$ when designated by an ITB modifier in the indirect word (m is an external ABR)
- $C(TBR)$ when brought in as a result of an ITS modifier in the indirect word

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.0 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh.A189 Sh. No.A188

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Control-Conditional Transfer		
TRC	TRANSFER ON CARRY	603 ₈

Summary: If Carry indicator ON, then $EA \Rightarrow C(ICTC)$, $C(TBR) \Rightarrow C(PBR)$

Description: The new Effective Address replaces the $C(ICTC)$, and the new Pointer in TBR formed during the Appending process for the transfer address replaces $C(PBR)$.
Pointers in TBR may come from the following sources:

- $C(PBR)$ when bit 29 of instruction word = 0
- $C(ABR_m)$ when bit 29 of instruction word = 1 (m is an external ABR)
- $C(ABR_m)$ when designated by an ITB modifier in the indirect word (m is an external ABR)
- $C(TBR)$ when brought in as a result of an ITS modifier in the indirect word

Modifications: All except DU, CL, CI, SC, SCR.

Timing: 2.0 μ sec

Indicators Affected: None

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Spec. No. M50EB0Q107
Cont. on Sh. A190 Sh. No. A189

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Control-Conditional Transfer

TNC	TRANSFER ON NO CARRY	602 ₈
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Summary: If Carry indicator OFF, then $EA \Rightarrow C(ICTC)$, $C(TBR) \Rightarrow C(PBR)$

Description: The new Effective Address replaces the $C(ICTC)$, and the new Pointer in TBR formed during the Appending process for the transfer address replaces $C(PBR)$. Pointers in TBR may come from the following sources:

- $C(PBR)$ when bit 29 of instruction word = 0
- $C(ABR_m)$ when bit 29 of instruction word = 1 (m is an external ABR)
- $C(ABR_m)$ when designated by an ITB modifier in the indirect word (m is an external ABR)
- $C(TBR)$ when brought in as a result of an ITS modifier in the indirect word

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.0 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh.A191 Sh. No.A190

TITLE: ENGINEERING PRODUCT SPECIFICATION
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Control-Conditional Transfer

TOV

TRANSFER ON OVERFLOW

617₈

Summary: If Overflow indicator ON, then $EA \Rightarrow C(ICTC)$, $C(TBR) \Rightarrow C(PBR)$

Description: The new Effective Address replaces the $C(ICTC)$, and the new Pointer in TBR formed during the Appending process for the transfer address replaces $C(PBR)$.
Pointers in TBR may come from the following sources:

- $C(PBR)$ when bit 29 of instruction word = 0
- $C(ABR_m)$ when bit 29 of instruction word = 1
(m is an external ABR)
- $C(ABR_m)$ when designated by an ITB modifier in the indirect word (m is an external ABR)
- $C(TBR)$ when brought in as a result of an ITS modifier in the indirect word

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.0 μ sec

Indicators Affected:

Overflow	Set OFF
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TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Control-Conditional Transfer

TEO

TRANSFER ON EXPONENT OVERFLOW

614₈

Summary: If Exponent Overflow indicator ON,
then $EA \Rightarrow C(ICTC)$; $C(TBR) \Rightarrow C(PBR)$

Description: The new Effective Address replaces the $C(ICTC)$, and the new Pointer in TBR formed during the Appending process for the transfer address replaces $C(PBR)$.
Pointers in TBR may come from the following sources:

- $C(PBR)$ when bit 29 of instruction word = 0
- $C(ABR_m)$ when bit 29 of instruction word = 1
(m is an external ABR)
- $C(ABR_m)$ when designated by an ITB modifier in the indirect word (m is an external ABR)
- $C(TBR)$ when brought in as a result of an ITS modifier in the indirect word

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.0 μ sec

Indicators Affected:

Exponent Overflow	Set OFF
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Spec. No. M50EB00107

Cont. on Sh. A193 Sh. No. A192

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Control-Conditional Transfer

TEU TRANSFER ON EXPONENT UNDERFLOW 615₈

Summary: If Exponent Underflow indicator ON,
then $EA \Rightarrow C(ICTC)$; $C(TBR) \Rightarrow C(PBR)$

Description: The new Effective Address replaces the $C(ICTC)$, and the new Pointer in TBR formed during the Appending process for the transfer address replaces $C(PBR)$. Pointers in TBR may come from the following sources:

- $C(PBR)$ when bit 29 of instruction word = 0
- $C(ABR_m)$ when bit 29 of instruction word = 1 (m is an external ABR)
- $C(ABR_m)$ when designated by an ITB modifier in the indirect word (m is an external ABR)
- $C(TBR)$ when brought in as a result of an ITS modifier in the indirect word

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.0 μ sec

Indicators Affected:

Exponent Underflow	Set OFF
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Spec. No. M50EB00107

Cont. on Sh.A194 Sh. No.A193

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Control-Conditional Transfer		
TTF	TRANSFER ON TALLY RUNOUT INDICATOR OFF	607 ₈

Summary: If Tally Runout indicator OFF, then $EA \Rightarrow C(ICTC)$; $C(TBR) \Rightarrow C(PBR)$

Description: The new Effective Address replaces the $C(ICTC)$, and the new Pointer in TBR formed during the Appending process for the transfer address replaces $C(PBR)$. Pointers in TBR may come from the following sources:

- $C(PBR)$ when bit 29 of instruction word = 0
- $C(ABR_m)$ when bit 29 of instruction word = 1 (m is an external ABR)
- $C(ABR_m)$ when designated by an ITB modifier in the indirect word (m is an external ABR)
- $C(TBR)$ when brought in as a result of an ITS modifier in the indirect word

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.0 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A195 Sh. No. A194

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		<u>Special</u>
CAM	CLEAR ASSOCIATIVE MEMORY	532 ₈

Summary: $0 \Rightarrow C(AR)_{54}$; usage value (0000-1111) $\Rightarrow C(AR)_{56-59}$
for all 16 AR's

Description: Execution of the CAM instruction sets the empty/full bit in each AR to zero, that is, empty, and initializes the usage value of each AR by arbitrarily assigning a unique number in the range 0-15 to each register. If this instruction is attempted in Slave mode an Illegal Procedure Fault will be generated.

Modifications: None can take place

Timing: 1.99 usec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh.A196 Sh. No.A195

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Special
BCD	BINARY TO BINARY-CODED-DECIMAL	505 ₈

Summary: $C(A) \div C(Y) \Rightarrow$ 4-bit quotient and remainder. Shift $C(Q)$ left six positions; 4-bit quotient $\Rightarrow C(Q)_{68-71}$ and remainder $\Rightarrow C(A)$. Shift $C(A)$ left three positions.

Description: This instruction carries out one step in an algorithm for the conversion of a number from the binary to the decimal system of notation, which requires the repeated short division of the binary number or last remainder by certain constants.

$$C_i = 8^i \times 10^{n-1} \text{ (for } i=1,2,\dots)$$

with N being defined by:

$$10^{n-1} \leq |\text{number}| \leq 10^n - 1$$

Modifications: All types except IT categories CI, SC, SCR.

Timing: 3.71 μ sec

Indicators Affected:

Zero	If $C(A) = 0$, then ON
Negative	If before execution $C(A)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A197 Sh. No. A196

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

GTB	GRAY TO BINARY	Special 774 ₈
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Summary: C(A) converted from Gray Code to binary representation
 $\Rightarrow C(A)$

Description: This conversion is defined by the following algorithm
where R_i and S_i denote the contents of bit positions i
of the A-register before and after conversion.

$$S_0 = R_0$$

$$S_i = (R_i \text{ AND } \overline{S_{i-1}}) \text{ OR } (\overline{R_i} \text{ AND } S_{i-1})$$

for $i=1,2,\dots,35$.

Modifications: Have no effect.

Timing: 9.87 μ sec

Indicators Affected:

Zero	If $C(A) = 0$, then ON; otherwise OFF
Negative	If $C(A)_0 = 1$, then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh. A198 Sh. No. A197

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Special
CIOC	CONNECT I/O CHANNEL	015 ₈

Summary: C(Y) are transferred from the memory module via the memory module port that is specified by C(Y).

- Description:
- 1) The absolute address Y is used to access a memory location as usual. However, the Memory module does not transmit the contents of this location to the Processor that submitted the absolute address; it uses C(Y)_{33...35} to select one of its eight ports, sends a connect pulse to the unit on this port, and then transmits C(Y) on the data lines to this unit. C(Y) must be a 0 mod. 8 address to be independent of interlace.
 - 2) This instruction can be used in the Master Mode only, and only by the Processor which has been designated the Control Processor for the accessed Memory module. If the use of this instruction is attempted by a Processor that is in the Slave Mode or that is not the Control Processor, an Illegal Memory Command Fault will occur.
 - 3) A CON command is sent out that Processor port selected by the 24 bit absolute address formed by this instruction.

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 1.35 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A199 Sh. No. A198

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Special
DIS	DELAY UNTIL INTERRUPT SIGNAL	6168

Summary: No operation takes place and the Processor waits for a program interrupt signal before continuing with the next instruction.

Description: This instruction may be executed in Master mode only or a 635/645 compatibility Fault trap will occur.

Modifications: Have no affect on the operation

Timing:

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A200 Sh. No. A199

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Special
DRL	DERAIL	002 ₈

Summary: Causes a fault which obtains and executes in the Absolute mode the two instructions stored at memory locations $4 + C$ and $5 + C$ decimal; the constant C being set up in the Maintenance Panel FAULT VECTOR switches.

Description: Execution of the DRL instruction implies the following conditions:

- 1) During the execution of this DRL instruction and the two instructions obtained, the Processor is in the Absolute mode, independent of the value of its Absolute indicator. The Processor will stay in the Absolute mode, if the Absolute indicator is ON after the execution of these three instructions.
- 2) The instruction from $4 + C$ must not alter the memory location $5 + C$, and must not be an XED instruction.
- 3) If the instruction from $4 + C$ alters the contents of the Instruction Counter, then this transfer of control is effective immediately; and the instruction from $5 + C$ is not executed.
- 4) After the execution of the two instructions obtained from Y-pair, the next instruction to be executed is obtained from $C(ICTC) + 1$. This is the instruction stored in the memory right after this DRL instruction unless the contents of the Instruction Counter have been changed by the execution of the two instructions obtained from $4 + C$ and $5 + C$.

Modifications: All types except CI, SC, SCR.

Timing: 2.0 μ sec

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Spec. No. M50EB00107

Cont. on Sh.A201 Sh. No.A200

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

DRL	DERAIL cont.	Special 002 ₈
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Indicators Affected: The DRL instruction itself does not affect any indicator. However, the execution of the two instructions from 4 + C and 5 + C may affect indicators; particularly, each one in turn will affect the Absolute Mode indicator as follows:

Absolute Mode	If the instruction obtained actually results in a transfer of control and is not the TSS instruction, then ON If the instruction obtained is either the RET or RTCD instruction with bit 29 = zero or the TSS instruction, then OFF
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Spec. No. M50EB00107

Cont. on Sh.A202 Sh. No.A201

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Special
MME	MASTER MODE ENTRY 1	001 ₈

Summary: Causes a fault which obtains and executes in the Absolute mode the two instructions stored at the memory locations $2 + C$ and $3 + C$ (decimal); the constant C is set up on the Maintenance Panel FAULT VECTOR switches.

Description: Execution of the MME instruction implies the following conditions:

- 1) During the execution of this MME instruction and the two instructions obtained, the Processor is in the Absolute mode independent of the value of its Absolute Mode indicator. The Processor will stay in Absolute mode if the Absolute Mode indicator is set ON after the execution of these three instructions.
- 2) The instruction from $2 + C$ must not alter the memory location $3 + C$, and must not be an XED instruction.
- 3) If the instruction from $2 + C$ alters the contents of the Instruction Counter, then this transfer of control is effective immediately and the instruction from $3 + C$ is not executed.
- 4) After the execution of the two instructions obtained from Y-pair, the next instruction to be executed is obtained from $C(ICTC) + 1$. This is the instruction stored in memory right after this MME instruction unless the contents of the Instruction Counter have been changed by the execution of the two instructions obtained from $2 + C$ and $3 + C$.

Modification: All types except CI, SC, SCR.

Timing: 2.0 μ sec

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Spec. No. M50EB00107

Cont. on Sh.A203 Sh. No. A202

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

MME	MASTER MODE ENTRY 1 cont.	Special 001 ₈
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Indicators Affected: The MME instruction itself does not affect any indicator. However, the execution of the two instructions from 2 + C and 3 + C may affect indicators; particularly, each one in turn will affect the Absolute Mode indicator as follows:

Absolute Mode	If the instruction obtained actually results in a transfer of control and is not the TSS instruction, then ON If the instruction obtained is either the RET or RTCD instruction with bit 29 = zero or the TSS instruction, then OFF
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Spec. No. M50EB00107

Cont. on Sh. A204 Sh. No. A203

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Special
MME2	MASTER MODE ENTRY 2	004 ₈

Summary: Causes a fault which obtains and executes in the Absolute mode the two instructions stored at the memory locations $8 + C$ and $9 + C$ (decimal); the constant C is set up on the Maintenance Panel FAULT VECTOR switches.

Description: Execution of the MME2 instruction implies the following conditions:

- 1) During the execution of this MME2 instruction and the two instructions obtained, the Processor is in the Absolute mode independent of the value of its Absolute Mode indicator. The Processor will stay in Absolute mode if the Absolute Mode indicator is set ON after the execution of these three instructions.
- 2) The instruction from $8+C$ must not alter the memory location $9+C$, and must not be an XED instruction.
- 3) If the instruction from $8+C$ alters the contents of the Instruction Counter, then this transfer of control is effective immediately and the instruction from $9+C$ is not executed.
- 4) After the execution of the two instructions obtained from Y-pair, the next instruction to be executed is obtained from $C(ICTC)+1$. This is the instruction stored in memory right after this MME2 instruction unless the contents of the Instruction Counter have been changed by the execution of the two instructions obtained from $8+C$ and $9+C$.

Modifications: All types except CI, SC, SCR.

Timing: 2.0 μ sec

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Spec. No. M50EB00107

Cont. on Sh. A205 Sh. No. A204

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

MME2

MASTER MODE ENTRY 2 cont.

Special

004₈

Indicators Affected: The MME2 instruction itself does not affect any indicator. However, the execution of the two instructions from 8+C and 9+C may affect indicators, particularly each one in turn will affect the Absolute Mode indicator as follows:

Absolute Mode	If the instruction obtained actually results in a transfer of control and is not the TSS instruction, then ON. If the instruction obtained is either the RET or RTCD instruction with bit 29 = zero or the TSS instruction, then OFF.
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Spec. No. M50EB00107
Cont. on Sh.A206 Sh. No.A205

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Special
MME3	MASTER MODE ENTRY 3	005 ₈

Summary: Causes a fault which obtains and executes in the Absolute mode the two instructions stored at the memory locations 10+C and 11+C (decimal); the constant C is set up on the Maintenance Panel FAULT VECTOR switches.

Description: Execution of the MME3 instruction implies the following conditions:

- 1) During the execution of this MME3 instruction and the two instructions obtained, the Processor is in the Absolute mode independent of the value of its Absolute Mode indicator. The Processor will stay in Absolute mode if the Absolute Mode indicator is set ON after the execution of these three instructions.
- 2) The instruction from 10+C must not alter the memory location 11+C and must not be an XED instruction.
- 3) If the instruction from 10+C alters the contents of the Instruction Counter, then this transfer of control is effective immediately and the instruction from 11+C is not executed.
- 4) After the execution of the two instructions obtained from Y-pair, the next instruction to be executed is obtained from C(ICTC)+1. This is the instruction stored in memory right after this MME3 instruction unless the contents of the Instruction Counter have been changed by the execution of the two instructions obtained from 10+C and 11+C.

Modifications: All types except CI, SC, SCR.

Timing: 2.0 μ sec

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Spec. No. M50EB00107

Cont. on Sh. A207 Sh. No. A206

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

MME3	MASTER MODE ENTRY 3	Special 005 ₈
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Indicators Affected: The MME3 instruction itself does not affect any indicator. However, the execution of the two instructions from 10+C and 11+C may affect indicators, particularly each one in turn will affect the Absolute Mode indicator as follows:

Absolute Mode	If the instruction obtained actually results in a transfer of control and is not the TSS instruction, then ON. If the instruction obtained is either the RET or RTCD instruction with bit 29 = zero or the TSS instruction, then OFF
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TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Special
MME4	MASTER MODE ENTRY 4	007 ₈

Summary: Causes a fault which obtains and executes in the Master mode the two instructions stored at the memory locations 14+C and 15+C (decimal); the constant C is set up on the Maintenance Panel FAULT VECTOR switches.

Description: Execution of the MME4 instruction implies the following conditions:

- 1) During the execution of this MME4 instruction and the two instructions obtained, the Processor is in the Absolute mode independent of the value of its Absolute Mode indicator. The Processor will stay in Absolute mode if the Absolute Mode indicator is set ON after the execution of these three instructions.
- 2) The instruction from 14+C must not alter the memory location 15+C, and must not be an XED instruction.
- 3) If the instruction from 14+C alters the contents of the Instruction Counter, then this transfer of control is effective immediately and the instruction from 15+C is not executed.
- 4) After the execution of the two instructions obtained from Y-pair, the next instruction to be executed is obtained from C(ICTC)+ 1. This is the instruction stored in memory right after this MME4 instruction unless the contents of the Instruction Counter have been changed by the execution of the two instructions obtained from 14+C and 15+C.

Modifications: All types except CI, SC, SCR.

Timing: 2.0 μ sec

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Spec. No. M50EB00107

Cont. on Sh. A209 Sh. No. A208

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Special
MME4	MASTER MODE ENTRY 4 cont.	007 ₈

Indicators Affected: The MME4 instruction itself does not affect any indicator. However, the execution of the two instructions from 14+C and 15+C may affect indicators, particularly each one in turn will affect the Absolute Mode indicator as follows:

Absolute Mode	If the instruction obtained actually results in a transfer of control and is not the TSS instruction, then ON If the instruction obtained is either the RET or RTCD instruction with bit 29 = zero or the TSS instruction, then OFF
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Spec. No. M50EB00107
Cont. on Sh. A210 Sh. No. A209

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Special
XEC	EXECUTE	716 ₈

Summary: Obtain and execute the instruction stored at the memory location Y.

Description: After the execution of the instruction obtained from location Y, the next instruction to be executed is obtained from C(ICTC)+ 1; the memory location immediately after the XEC instruction unless the contents of the instruction counter have been changed by the execution of the instruction obtained from location Y.

To execute (XEC) a Repeat Double (RPD) instruction, the XEC instruction must be in an odd location.

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.0 μ sec

Indicators Affected: The XEC instruction itself does not affect any indicators. However, the execution of the instruction from Y may affect indicators.

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Spec. No. M50EB00107

Cont. on Sh. A211 Sh. No. A210

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Special
XED	EXECUTE DOUBLE	717 ₈

Summary: Obtain and execute the two instructions stored at the memory location Y-pair.

Description: Execution of the XED instruction implies the following conditions:

- 1) The first instruction obtained from the Y-pair must not alter the memory location from which the second instruction is obtained and must not be another XED instruction.
- 2) If the first instruction obtained from the Y-pair alters the contents of the Instruction Counter, then this transfer of control is effective immediately and the second instruction of the pair is not executed.
- 3) After execution of the two instructions obtained from the Y-pair, the next instruction to be executed is obtained from C(ICTC)+1, the memory location immediately after the XED instruction, unless the contents of the Instruction Counter have been changed by the execution of the two instructions obtained from the memory locations of the Y-pair.
- 4) To Execute Double (XED) a pair which has Repeat Double (RPD) as the odd instruction of the pair, XED must be located at the odd address.

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.0 μ sec

Indicators Affected: The XED instruction does not affect any indicator. However, the execution of the two instructions from the Y-pair may affect indicators.

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Special

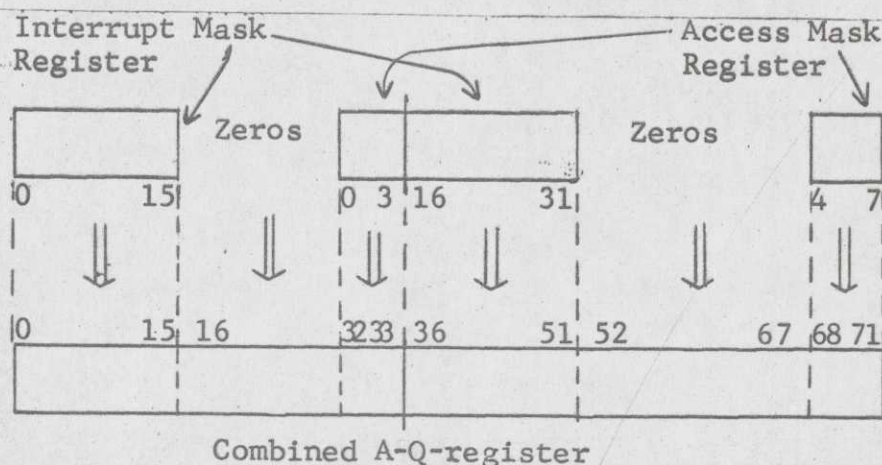
RMCM

READ MEMORY CONTROLLER MASK REGISTER

233₈

Summary: C(Memory Controller Interrupt Mask Register) $\Rightarrow$ C(AQ)
 C(Memory Controller Access Mask Register)
 of Memory Unit specified.

Description: 1) The absolute address generated for this instruction is used in selecting a Processor port as with a normal memory access request. However, the selected module does not transmit the contents of the addressed memory location, but the contents of its Memory Controller Interrupt Mask Register and Memory Controller Access Mask Register.



2) When selecting a memory module; memory size, instruction word address field, PBR, TBR, internal and external ABR's, and memory interlace (if the final address is not 0 mod 8) must be considered. See the Address Modification flow chart Fig. 2.6.2 for address development.

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Spec. No. M50EB00107

Cont. on Sh.A213 Sh. No. A212

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

- 3) This instruction can be used in the Master mode only. If the use of this instruction is attempted by a Processor that is in the Slave mode a 635/645 Compatibility Fault will occur.
- 4) The memory command actually sent out the Processor port is RMSK.

Modifications: All types except DU, DL, CI, SC, SCR.

Timing: 1.35 μ sec

Indicators Affected:

Zero	If $C(AQ) = 0$, then ON; otherwise OFF
Negative	If $C(AQ)_0 = 1$, then ON; otherwise OFF

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Special

SMCM

SET MEMORY CONTROLLER MASK REGISTER

553₈

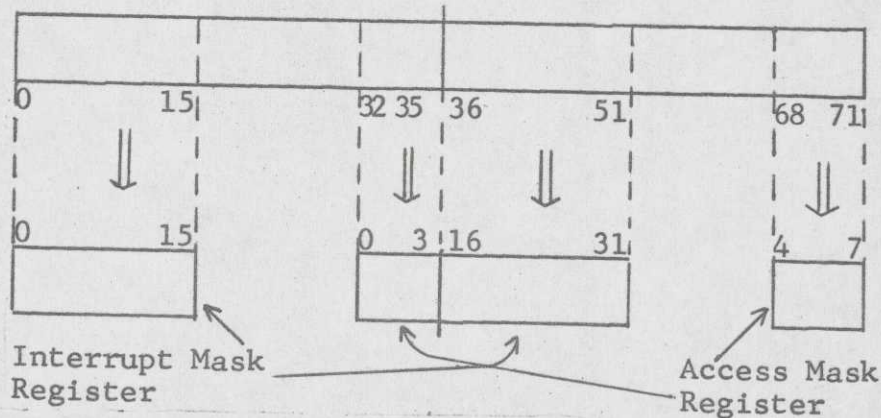
Summary:

C(AQ) = C(Memory Controller Interrupt Mask Register)
 C(Memory Controller Access Mask Register)
 of Memory Unit specified.

Description:

- 1) The absolute address generated for this instruction is used in selecting a Processor port as with a normal memory access request. However, the selected module does not store the data received in a memory location, but in its Memory Controller Interrupt Mask Register and Memory Controller Access Mask Register.

Combined AQ-register



- 2) When selecting a memory module; memory size, instruction word address field, PBR, TBR, internal and external ABR's, and memory interlace (if the final address is not 0 mod 8) must be considered. See the Address Modification flow chart Fig. 2.6.2 for Address development.

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Spec. No. M50EB00107

Cont. on Sh. A215 Sh. No. A214

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

- 3) This instruction can be used in the Master mode only. If the use of this instruction is attempted by a Processor that is in the Slave mode a 635/645 Compatibility Fault will occur.
- 4) The command actually sent out the Processor port is SMSK.

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 3.97 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh. A216 Sh. No. A215

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Special

SMIC

SET MEMORY CONTROLLER INTERRUPT CELLS

451₈

Summary: C(A) is used to set selected Interrupt Cells ON in the Memory Controller of the memory unit selected.

- Description: 1) The absolute address generated for this instruction is used in selecting a Processor port as with a normal memory access request. However, the selected module does not store the data received in a memory location, but uses it to set selected Interrupt Cells ON.
- For $i=0,1,\dots,15$ AND $C(A)_{35} = 0$: if $C(A)_i = 1$;
then set Interrupt Cell_i ON
- For $i=0,1,\dots,15$ AND $C(A)_{35} = 1$: if $C(A)_i = 1$;
then set Interrupt Cell (16+i) ON
- 2) When selecting a memory module; memory size, instruction word address field, PBR, TBR, internal and external ABR's, and memory interlace (if the final address is not 0 mod 8) must be considered. See the Address Modification flow chart Fig. 2.6.2 for Address development.
- 3) This instruction can be used in the Master mode only or a 635/645 Compatibility Fault Trap will occur.
- 4) The command actually sent out the Processor port is SXC.

Modifications: All except DU, DL, CI, SC, SCR.

Timing: 2.0 μ sec

Indicators Affected: None

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

		Special
RPT	REPEAT	520 ₈

Summary: Execute the next instruction a specified number of times or until a specified Terminate condition is met.

Description: 1) This RPT instruction has the following format:

0	7	8	9	10	11	17	18	26	27	28	29	30	35
Tally	~	~	C	Term.Cond.	Op Code	0	1	0	Delta				

- 2) If C = 1, then bits 0-17 of the RPT instruction $\Rightarrow$ X0. If C = 0, then X0 contains whatever was left from the previous instruction.
- 3) In any case, the Terminate condition and Tally from X0 will control the repetition loop for the instruction following this RPT instruction; initial Tally = 0 will be interpreted as 256.
- 4) The repetition loop consists of the following steps:
 - a) Execute the repeated instruction,
 - b) $C(X0)_{0...7-1} \Rightarrow C(X0)_{0...7}$
 - c) If Termination condition met (see 7), then terminate,
 - d) If $C(X0)_{0...7}=0$, then set Tally Runout indicator ON and terminate:
 - e) Go to 4a.
- 5) All instructions can be used as repeated instructions except the following:
 - a) All control instructions
 - b) All special instruction operations except BCD
 - c) All general base instructions--LBRm, EABm, ADBm, SBRm, LDBR, CAM, EAPm, LDCF, RTD, STCD, STPm, ZAM, TSBm, SCU, RCU, LDB
- 6) Address modification for the repeated instruction:
 For the repeated instruction, only the modifiers R and RI are permitted, and only the designators specifying X1,...,X7. The effective address EA (in the case of R) or the address EA of the indirect word to be referenced (in the case of RI) will be:

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Spec. No. M50EB00107

Cont. on Sh. A218 Sh. No. A217

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

RPT	REPEAT cont.	Special
		520 ₈
	a) For the <u>first execution</u> of the repeated instruction	
	$y + C(R) \Rightarrow EA, EA \Rightarrow C(R)$	
	b) For <u>any successive execution</u>	
	$C(R) + \Delta \Rightarrow EA, EA \Rightarrow C(R)$	
	In the case of RI, only one indirect reference will be made per repeated execution. The tag portion of the indirect word will not be interpreted as usual, but will be ignored; and instead the modifier R and the designator R = N will be applied.	
	7) The Terminate conditions:	
	The possible Terminate conditions are the same for all three repeat instructions-- RPT, RPD, RPL, except that RPL can terminate on a link address = 0.	
	The bit configuration in bit positions 11-17 of the RPT instruction defines the Terminate conditions for which the repetition loop will be terminated immediately. If more than one condition is specified, the repeat will terminate if any of the specified conditions are met.	
	Bit 17 = 0 : any overflow is completely ignored, that is, neither the respective Overflow indicator is set ON, nor an Overflow Trap occurs.	
	= 1 : any overflow terminates the repetition loop, and it is treated as usual; that is, the respective Overflow indicator is set ON, and if the Overflow Mask indicator is OFF, then an Overflow Fault Trap occurs.	
	Bit 16 = 1 : if Carry indicator is OFF, then terminate the repetition loop.	

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Spec. No. M50EB00107

Cont. on Sh. A219 Sh. No. A218

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

RPT	REPEAT cont.	Special
		5208
	Bit 15 = 1 : if Carry indicator is ON, then terminate the repetition loop. Bit 14 = 1 : if Negative indicator is OFF, then terminate the repetition loop. Bit 13 = 1 : if Negative indicator is ON, then terminate the repetition loop. Bit 12 = 1 : if Zero indicator is OFF, then terminate the repetition loop. Bit 11 = 1 : if Zero indicator is ON, then terminate the repetition loop. A "0" in both bit positions for one indicator will cause this indicator to be ignored as a Terminate condition; a "1" in both bit positions will cause a termination after the first execution of the repeated instruction. 8) <u>At the time of termination:</u> X0...7 will contain the Tally Residue; that is, the number of repeats remaining until a Tally Runout would have occurred. If the RPT instruction is interrupted before termination, the Tally Runout indicator will be OFF in any case.	
	The Xn specified by the designator of the repeated instruction will contain the effective address of the next operand or indirect word that would have been secured (this is because of the overlap between an execution of the repeated instruction and the address modification for the next execution of the repeated instruction).	

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Spec. No. M50EB00107

Cont. on Sh. A220 Sh. No. A219

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Special
RPT	REPEAT cont.	520 ₈

Modifications: No modification can take place

Timing: 1.35 μ sec

Indicators Affected:

Tally Runout	If termination because of Tally = 0, then ON If because Terminate condition is met, then OFF
All other indicators	The RPT instruction itself does not affect any of the other indicators. However, the execution of the repeated instruction may affect indicators.

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Spec. No. M50EB00107
Cont. on Sh. A221 Sh. No. A220

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Special

RPD

REPEAT DOUBLE

Summary: Execute the pair of instructions from the next location
Y-pair a specified number of times or until a specified
Terminate condition is met.

- Description: 1) The RPD instruction must be stored in an odd
memory location except when accessed via the
XEC instruction in which case the RPD instruc-
tion can be either even or odd.
- 2) This RPD instruction has the following format:

0	7	8	9	10	11	17	18	26	27	28	29	30	35
Tally	A	B	C	Term.Cond.			Op.Code	0	1	0	Delta		

- 3) If C = 1, then bits 0-17 of the RPD instruction $\Rightarrow$ XO
If C = 0, then XO contains whatever was left from
the previous instruction.
- 4) In any case, the Terminate condition and Tally from
XO will control the repetition loop for the instruc-
tion following this RPD instruction; initial Tally =
0 will be interpreted as 256.
- 5) The repetition cycle consists of the following steps:
- Execute the pair of repeated instructions
 - $C(XO)_{0..7-1} \Rightarrow C(XO)_{0..7}$
 - If Termination condition met after termination of
odd instruction, (see 8), then terminate.
 - If $C(XO)_{0..7} = 0$, then set Tally Runout indicator
ON and terminate.
 - Go to 5a.

Note that if an Overflow Fault occurs on the even
instruction, this precludes execution of the odd
instruction.

- 6) All instructions can be used as repeated instruc-
tions except the following:
- All control instructions.
 - All special operations instructions
except BCD.
 - All general base instructions--LBRm, EABm, ADBm,
SBRm, LDBR, SDBR, CAM, EAPm, LDCF, RTD, STCD,
STPm, ZAM, TSBm, SCU, RCU, LDB, STB, SAM.

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Spec. No. M50EB00107
Cont. on Sh. A222 Sh. No. A221

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Special

RPD

REPEAT DOUBLE cont.

560₈

7) Address Modification for the pair of repeated instructions:

For each of the two repeated instructions, only the modifiers R and RI are permitted, and only the designators specifying X1,...,X7.

The effective address EA (in the case of R) or the address EA of the indirect word to be referenced (in the case of RI) will be:

a) For the first execution of each of the two repeated instructions

$$y + C(R) \Rightarrow EA, EA \Rightarrow C(R)$$

b) For any successive execution of

The first of the two repeated instructions

if A = 1, then $C(R) + \Delta \Rightarrow EA, EA \Rightarrow C(R)$ or
if A = 0, then $C(R) \Rightarrow EA$

The second of the two repeated instructions

if B = 1, then $C(R) + \Delta \Rightarrow EA, EA \Rightarrow C(R)$ or
if B = 0, then $C(R) \Rightarrow EA$

(A and B being the contents of bit positions 8 and 9 of the RPD instruction)

In the case of RI, only one indirect reference will be made per repeated execution. The Tag portion of the indirect word will not be interpreted as usual, but will be ignored; and instead the modifier R and the designator R=N will be applied.

8) The Terminate conditions:

The possible Terminate conditions are the same for all three repeat instructions - RPT, RPD, RPL except that RPL may be terminated on a link address = 0.

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Spec. No. M50EB00107
Cont. on Sh.A223 Sh. No. A222

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Special
RPD	REPEAT DOUBLE cont.	560g
	The bit configuration in bit positions 11-17 of the RPD instruction defines the Terminate conditions for which the repetition loop will be terminated upon completion of the odd instruction. If more than one condition is specified, the repeat will terminate if any of the specified conditions are met. Bit 17 = 0 : any overflow is completely ignored, that is, neither the respective Overflow indicator is set ON, nor an Overflow Trap occurs. = 1 : any overflow terminates the repetition loop, and it is treated as usual; that is, the respective Overflow indicator is set ON, and if the Overflow Mask is OFF, then also an Overflow Fault Trap occurs. If the Overflow Fault Trap occurs on the even instruction, the odd instruction is not executed. Bit 16 = 1 : if Carry indicator is OFF, then terminate the repetition loop. Bit 15 = 1 : if Carry indicator is ON, then terminate the repetition loop. Bit 14 = 1 : if Negative indicator is OFF, then terminate the repetition loop. Bit 13 = 1 : if Negative indicator is ON, then terminate the repetition loop. Bit 12 = 1 : if Zero indicator is OFF, then terminate the repetition loop. Bit 11 = 1 : if Zero indicator is ON, then terminate the repetition loop.	

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Spec. No. M50EB00107
Cont. on Sh. A224 Sh. No. A223

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

RPD	REPEAT DOUBLE cont.	Special 560 ₈
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9) At the time of termination:

X0_{0...7} will contain the Tally Residue, that is, the number of repeats remaining until a Tally Runout would have occurred.

If the RPD instruction is interrupted before Termination, the Tally Runout indicator will be OFF in any case.

The Xn specified by the designator of each of two repeated instructions will contain the effective address of the next operand or indirect word that would have been secured (special provisions have been made that this statement is true for both of the repeated instructions).

Modifications: None can take place.

Timing: 1.35 μ sec

Indicators Affected:

Tally Runout	If termination because of Tally = 0, then ON If because Terminate condition is met, then OFF.
All other indicators	The RPD instruction itself does not affect any of the other indicators. However, the execution of the repeated instructions may affect indicators.

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Spec. No. M50EB00107

Cont. on Sh. A225 Sh. No. A224

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Special

RPL

REPEAT LINK

500₈

Summary: Execute the next instruction a specified number of times, until a specified Terminate condition is met or a Link Address Zero is found.

Description: 1) This RPL instruction has the following format:

0	7	8	9	10	11	17	18	26	27	28	29	30	35
Tally	~	~		C	Term.Cond.	Op.Code	0	1	0				

- 2) If $C = 1$, then bits 0-17 of the RPL instruction $\Rightarrow$ XO. If $C = 0$ the XO contains whatever was left from the previous instruction.
 - 3) In any case, the Terminate condition and Tally from XO will control the repetition loop for the instruction following this RPL instruction; initial Tally = 0 will be interpreted as 256.
 - 4) The repetition loop consists of the following steps:
 - a) Execute the repeated instruction
 - b) $C(XO)_0 \dots 7 \Rightarrow C(XO)_0 \dots 7$
 - c) If Termination condition met (see 7), then set Tally Runout indicator OFF and terminate
 - d) If the Tally $C(Xn)_0 \dots 17 = 0$ or the Link Address $C(Y)_0 \dots 17 = 0$, then set Tally Runout indicator ON and terminate
- NOTE:
- If first address is zero; termination will result upon completion of the first operation.
- e) Go to 4a.

5) All instructions can be used as repeated instructions except the following:

- a) Instructions that could alter the Link Address $C(Y)_0 \dots 17$
- b) EAA, EAQ, EAX, NEG, NEGL
- c) All special operations instructions
- d) All shift instructions
- e) All control instructions
- f) All general base instructions --LBRn, EABn, ADBn, SBRn, LDBR, SDBR, CAM, EAPn, LDCF, RTD, STCD, STPn, ZAM, TSBn, SCU, RCU, LDB, STB, SAM.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Special

RPL

REPEAT LINK cont.

500₈

6) Address modification for the repeated instruction:

For the repeated instruction, only the modifier R is permitted, and only the designators specifying $R = X1, \dots, X7$.

The effective address EA will be

For the first execution of the repeated instruction

$y + C(R) \Rightarrow EA$; y of word fetched $\Rightarrow C(R)$

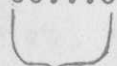
For any successive execution of the repeated instruction

$C(R) \Rightarrow EA$; y of word fetched $\Rightarrow C(R)$

The effective address EA is the address of the next list word.

The upper half of the list word contains the Link Address, that is, the address of the next successive list word, and thus the effective address for the next successive execution of the repeated instruction.

The lower half of this list word contains the operand to be used for this execution of the repeated instruction; the operand is

$00\dots0,$ $C(Y)_{18\dots35}$

18 times

For double-precision instructions that are being repeated; the operand is

$00\dots0,$ $C(Y)_{18-35}, C(Y+1)_{0-35}$

18 times

7) The Terminate conditions:

The possible Terminate conditions are the same for all three repeat instructions - RPT, RPD, RPL except that RPL can terminate on a Link Address = 0.

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Spec. No. M50EB00107

Cont. on Sh.A227 Sh. No. A226

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

RPL	REPEAT LINK	cont.	Special 500g
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The bit configuration in bit positions 11-17 of the RPL instruction defines the Terminate conditions for which the repetition loop will be terminated immediately. If more than one condition is specified, the repeat will terminate if any of the specified conditions are met.

Bit 17 = 0 : any overflow is completely ignored; that is, neither the respective Overflow indicator is set ON, nor an Overflow Trap occurs;

= 1 : any overflow terminates the repetition loop, and it is treated as usual; that is, the respective overflow indicator is set ON, and if the Overflow Mask indicator is OFF, then also an Overflow Fault Trap occurs.

Bit 16 = 1 : if Carry indicator is OFF, then terminate the repetition loop.

Bit 15 = 1 : if Carry indicator is ON, then terminate the repetition loop.

Bit 14 = 1 : if Negative indicator is OFF, then terminate the repetition loop.

Bit 13 = 1 : if Negative indicator is ON, then terminate the repetition loop.

Bit 12 = 1 : if Zero indicator is OFF, then terminate the repetition loop.

Bit 11 = 1 : if Zero indicator is ON, then terminate the repetition loop.

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Spec. No. M50EB00107
Cont. on Sh.A228 Sh. No.A227

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Special

RPL

REPEAT LINK cont.

500₈

8) At the time of termination:

X0_{0...7} will contain the Tally residue, that is, the numbers of repeats remaining until a Tally runout would have occurred. If the RPL instruction is interrupted before Termination, the Tally Runout indicator will be OFF in any case.

The Xn specified by the designator of this repeated instruction will contain the address of the list word that contains

In its upper half: the address of the next list word

In its lower half: the operand used in the last execution of the repeated instruction, for single-precision instructions. For double-precision instructions, this half word and the next full word are the operand last used.

(This is because there is no overlap between an execution of the repeated instruction and the address modification for the next execution of the repeated instruction.)

Modifications: No modification can take place

Timing: 1.35 μ sec

Indicators Affected:

Tally Runout	If termination because of Tally = 0 or Link Address = 0, then ON. If because Terminate condition is met, then OFF.
All other indicators	The RPL instruction itself does not affect any of the other indicators. However, the execution of the repeated instruction may affect indicators.

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Spec. No. M50EB00107

Cont. on Sh. A229 Sh. No. A228

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		Special
RSW	READ SWITCHES	231 ₈

Summary: C(Data Switches on Maintenance Panel) $\Rightarrow$ C(A)₀₋₃₅

Description:

Modifications: All types except DU, DL, CI, SC, SCR are allowed
but none effect the operation of RSW.

Timing: 1.35 μ sec

Indicators Affected:

Zero	if C(A) =0, Then ON; otherwise OFF
Negative	if C(A) ₀ =1, Then ON; otherwise OFF

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Spec. No. M50EB00107

Cont. on Sh.A230 Sh. No. A229

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

NOP	NO OPERATION	Special 011 ₈
-----	--------------	-----------------------------

Summary: No operation takes place

Description: No operation takes place but address modification may take place. If modification other than DU or DL is used, the effective address will be used in a memory access request which could lead to memory faults. The use of IT modification categories ID, DI, IDC, DIC causes the respective changes in the address and tally.

Modifications: Generally the modification N, DU or DL should be used.

Timing: 1.47 μ sec

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh.A231 Sh. No.A230

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Special

LACL

LOAD ALARM CLOCK

453₈

Summary: C(AQ)₂₀₋₆₅ ⇒ C(Alarm Clock)₅₁₋₆

- Description:
- 1) The Absolute address generated for this instruction is used in selecting a Processor Port as with a normal memory access request but execution requires only an address for port selection since this instruction involves a non-core memory command like the RCCL, RMCM, SMCM, and SMIC instructions.
 - 2) When selecting a memory module; memory size, instruction word address field, PBR, TBR, internal and external ABR's, and memory interlace (if the final address is not 0 mod 8) must be considered. See the Address Modification flow chart Fig. 2.6.2 for Address development.
 - 3) This instruction may be executed in Master Mode only or an Illegal Procedure Fault is generated.
 - 4) The command actually sent out the Processor port is SAC.

Modifications: All except DU, DL, CI, SC, SCR.

Timing:

Indicators Affected: None

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Spec. No. M50EB00107

Cont. on Sh.A232 Sh. No.A231

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Special

RCCL

READ CALENDAR CLOCK

633₈

Summary: $0...0 = C(AQ)_{0-19}; C(\text{Calendar Clock}) = C(AQ)_{20-71}$

- Description:
- 1) The absolute address generated for this instruction is used in selecting a Processor Port as with a normal memory access request but execution requires only an address for port selection, since this instruction involves a non-core memory command like the LACL, RMCM, SMCM and SMIC instructions.
 - 2) When selecting a memory module; memory size, instruction word address field, PBR, TBR, internal and external ABR's, and memory interlace (if the final address is not 0 mod 8) must be considered. See the Address Modification flow chart Fig. 2.6.2 for Address development.
 - 3) The Command actually sent out the Processor Port is RCC.

Modifications: All except DU, DL, CI, SC, SCR.

Timing:

Indicators Affected: None

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

A4 INDEX BY FUNCTIONAL CLASS

DATA MOVEMENT

<u>Load</u>		<u>Page</u>
EAA	635 Effective Address to Accumulator	A8
EAQ	636 Effective Address to Quotient Register	A9
EAXn	62n Effective Address to Index Register	A10
EABn	(310-313) Effective Address to Base n (330-333)	A11
EAPn	(350-313) Effective Address to Pair n (370-373)	A12
LBRn	76n Load Address Base Register n	A13
LDB	173 Load Bases	A14
LDBR	232 Load Descriptor Segment Base Register	A15
LDCF	512 Load Control Field	A16
LDA	235 Load Accumulator	A17
LDQ	236 Load Quotient Register	A18
LDAQ	237 Load A-Q Register	A19
LDT	637 Load Timer Register	A20
LDXn	22n Load Index Register n	A21
LXLn	72n Load Index Register n from lower	A22
LDI	634 Load Indicator Register	A23
LREG	073 Load Register	A24
LCA	335 Load Complement into Accumulator	A25
LCQ	336 Load Complement into Quotient Register	A26
LCAQ	337 Load Complement into A-Q Register	A27
LCXn	32n Load Complement into Index Register n	A28
<u>Store</u>		
SAM	557 Store Associative Memory	A29
ZAM	157 Store Associative Memory Zero	A30

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		<u>Page</u>
SBRn	54n Store Address Base Register n	A31
STB	254 Store Bases	A32
SDBR	154 Store Descriptor Segment Base Register	A33
STPn	(250-253) Store Pair n (650-653)	A34
STCD	357 Store Control Double	A35
STA	755 Store Accumulator	A36
STAC	354 Store A Conditional	A37
STQ	756 Store Quotient Register	A38
STAQ	757 Store A-Q Register	A39
STXn	74n Store Index Register n	A40
SXLn	44n Store Index Register n in Lower	A41
SREG	753 Store Registers	A42
STCA	751 Store Characters of Accumulator (6 bit)	A43
STCQ	752 Store Characters of Quotient Register (6 bit)	A44
STBA	551 Store Characters of Accumulator (9 bit)	A45
STBQ	552 Store Characters of Quotient Register (9 bit)	A46
STI	754 Store Indicator Register	A47
STT	454 Store Timer Register	A48
SCU	657 Store Control Unit	A49
STC1	554 Store Instruction Counter plus 1	A55
STC2	750 Store Instruction Counter plus 2	A56
STZ	450 Store Zero	A57
<u>Shift</u>		
ARS	731 Accumulator Right Shift	A58
QRS	732 Quotient Register Right Shift	A59
LRS	733 Long Right Shift	A60
ALS	735 Accumulator Left Shift	A61
QLS	736 Quotient Register Left Shift	A62
LLS	737 Long Left Shift	A63
ARL	771 Accumulator Right Logical	A64
QRL	772 Quotient Register Right Logical	A65

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		<u>Page</u>
LRL	773 Long Right Logical	A66
ALR	775 Accumulator Left Rotate	A67
QLR	776 Quotient Register Left Rotate	A68
LLR	777 Long Left Rotate	A69
FIXED-POINT ARITHMETIC		
<u>Addition</u>		
ADBn	(050-053) Add to Address Base Register n (150-153)	A70
ADA	075 Add to Accumulator	A71
ADQ	076 Add to Quotient Register	A72
ADAQ	077 Add to A-Q Register	A73
ADXn	06n Add to Index Register n	A74
ASA	055 Add Stored to Accumulator	A75
ASQ	056 Add Stored to Quotient Register	A76
ASXn	04n Add Stored to Index Register n	A77
ADLA	035 Add Logical to Accumulator	A78
ADLQ	036 Add Logical to Quotient Register	A79
ADLAQ	037 Add Logical to A-Q Register	A80
ADLXn	02n Add Logical to Index Register n	A81
AWCA	071 Add with Carry to Accumulator	A82
AWCQ	072 Add with Carry to Quotient Register	A83
ADL	033 Add Low to A-Q Register	A84
AOS	054 Add One to Storage	A85
<u>Subtraction</u>		
SBA	175 Subtract from Accumulator	A86
SBQ	176 Subtract from Quotient Register	A87

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

		<u>Page</u>
SBAQ	177 Subtract from A-Q Register	A88
SBXn	16n Subtract from Index Register n	A89
SSA	155 Subtract Stored from Accumulator	A90
SSQ	156 Subtract Stored from Quotient Register	A91
SSXn	14n Subtract Stored from Index Register n	A92
SBLA	135 Subtract Logical from Accumulator	A93
SBLQ	136 Subtract Logical from Quotient Register	A94
SBLAQ	137 Subtract Logical from A-Q Register	A95
SBLXn	12n Subtract Logical from Index Register n	A96
SWCA	171 Subtract with Carry from Accumulator	A97
SWCQ	172 Subtract with Carry from Quotient Register	A98
<u>Multiplication</u>		
MPY	402 Multiply Integer	A99
MPF	401 Multiply Fraction	A100
<u>Division</u>		
DIV	506 Divide Integer	A101
DVF	507 Divide Fraction	A102
<u>Negate</u>		
NEG	531 Negate Accumulator	A104
NEGL	533 Negate Long	A105
<u>Load</u>		
FLD	431 Floating Load	A106
DFLD	433 Double-precision Floating Load	A107
LDE	411 Load Exponent Register	A108
<u>Store</u>		
FST	455 Floating Store	A109
DFST	457 Double-Precision Floating Store	A110
STE	456 Store Exponent Register	A111

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

FLOATING-POINT ARITHMETIC

Page

Addition

FAD	475 Floating Add	A112
UFA	435 Unnormalized Floating Add	A113
DFAD	477 Double-Precision Floating Add	A114
DUFA	437 Double-Precision Unnormalized Floating Add	A115
ADE	415 Add to Exponent Register	A116

Subtraction

FSB	575 Floating Subtract	A117
UFS	535 Unnormalized Floating Subtract	A118
DFSB	577 Double-Precision Floating Subtract	A119
DUFS	537 Double-Precision Unnormalized Floating Subtract	A120

Multiplication

FMP	461 Floating Multiply	A121
UFM	421 Unnormalized Floating Multiply	A122
DFMP	463 Double-Precision Floating Multiply	A123
DUFM	423 Double-Precision Unnormalized Floating Multiply	A124

Division

FDV	565 Floating Divide	A125
FDI	525 Floating Divide Inverted	A126
DFDV	567 Double-Precision Floating Divide	A127
DFDI	527 Double-Precision Floating Divide Inverted	A128

Negate

FNEG	513 Floating Negate	A129
FNO	573 Floating Normalize	A130

Compare

FCMP	515 Floating Compare	A131
FCMG	425 Floating Compare Magnitude	A132

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

DFCMP	517 Double-Precision Floating Compare	A133
DFCMG	427 Double-Precision Floating Compare Magnitude	A134
FSZN	430 Floating Set Zero and Negative Indicators from Memory	A135

BOOLEAN OPERATIONS

AND

ANA	375 AND to Accumulator	A136
ANQ	376 AND to Quotient Register	A137
ANAQ	377 AND to A-Q Register	A138
ANXn	36n AND to Index Register n	A139
ANSA	355 AND to Storage Accumulator	A140
ANSQ	356 AND to Storage Quotient Register	A141
ANSXn	34n AND to Storage Index Register n	A142

OR

ORA	275 OR to Accumulator	A143
ORQ	276 OR to Quotient Register	A144
ORAQ	277 OR to A-Q Register	A145
ORXn	26n OR to Index Register n	A146
ORSA	255 OR to Storage Accumulator	A147
ORSQ	256 OR to Storage Quotient Register	A148
ORSXn	24n OR to Storage Index Register	A149

Exclusive OR

ERA	675 Exclusive OR to Accumulator	A150
ERQ	676 Exclusive OR to Quotient Register	A151
ERAQ	677 Exclusive OR to A-Q Register	A152
ERXn	66n Exclusive OR to Index Register n	A153
ERSA	655 Exclusive OR to Storage Accumulator	A154
ERSQ	656 Exclusive OR to Storage Quotient Register	A155
ERSXn	64n Exclusive OR to Storage Index Register n	A156

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

COMPARISON

Page

Compare

CMPA	115 Compare with Accumulator	A157
CM PQ	116 Compare with Quotient Register	A158
CM PAQ	117 Compare with A-Q Register	A159
CM PXn	10n Compare with Index Register n	A160
CWL	111 Compare with Limits	A161
CMG	405 Compare Magnitude	A162
SZN	234 Set Zero and Negative Indicators from Memory	A163
CMK	211 Compare Masked	A164

Comparative AND

CANA	315 Comparative AND with Accumulator	A165
CANQ	316 Comparative AND with Quotient Register	A166
CANAQ	317 Comparative AND with A-Q Register	A167
CANXn	30n Comparative AND with Index Register n	A168

Comparative NOT

CNAA	215 Comparative NOT with Accumulator	A169
CNAQ	216 Comparative NOT with Quotient Register	A170
CNAAQ	217 Comparative NOT with A-Q Register	A171
CNAXn	20n Comparative NOT with Index Register n	A172

CONTROL

Transfer

TRA	710 Transfer Unconditionally	A173
T SBn	(270-273) Transfer and Set Base n (670-673)	A174
T SXn	70n Transfer and Set Index Register n	A176
T SS	715 Transfer and Set Slave	A177

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Spec. No. M50EB00107

Cont. on Sh. A240 Sh. No. A239

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

RET	630 Return	A178
RTCD	610 Return Double	A179
RCU	613 Restore Control Unit	A180

Conditional Transfer

TZE	600 Transfer on Zero	A184
TNZ	601 Transfer on Not Zero	A185
TMI	604 Transfer on Minus	A186
TPL	605 Transfer on Plus	A187
TRC	603 Transfer on Carry	A188
TNC	602 Transfer on No Carry	A189
TOV	617 Transfer on Overflow	A190
TEO	614 Transfer on Exponent Overflow	A191
TEU	615 Transfer on Exponent Underflow	A192
TTF	607 Transfer on Tally-Runout Indicator OFF	A193

SPECIAL INSTRUCTIONS

CAM	532 Clear Associative Memory	A194
BCD	505 Binary to Binary-Coded-Decimal	A195
GTB	774 Gray to Binary	A196
CIOC	015 Connect Input/Output Channel	A197
DIS	616 Delay until Interrupt Signal	A198
DRL	022 Derail	A199
MME	001 Master Mode Entry 1	A201
MME2	004 Master Mode Entry 2	A203
MME3	005 Master Mode Entry 3	A205
MME4	007 Master Mode Entry 4	A207
XEC	716 Execute	A209
XED	717 Execute Double	A210

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Spec. No. M50EB00107

Cont. on Sh.A241 Sh. No. A240

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

RMC	233 Read Memory Controller Mask Registers	A211
SMC	553 Set Memory Controller Mask Registers	A213
SMIC	451 Set Memory Controller Interrupt Cells	A215
RPT	520 Repeat	A216
RPD	560 Repeat Double	A220
RPL	500 Repeat Link	A224
RSW	231 Read Switches	A228
NOP	011 No Operation	A229
LACL	453 Load Alarm Clock	A230
RCCL	633 Read Calendar Clock	A231

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Spec. No. M50EB00107

Cont. on Sh.A242 Sh. No.A241

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

A5 ALPHABETICAL INDEX

<u>MNEMONIC</u>	<u>Page</u>	<u>MNEMONIC</u>	<u>Page</u>	<u>MNEMONIC</u>	<u>Page</u>
ADA	A71	CMG	A162	ERSA	A154
ADAAQ	A73	CMK	A164	ERSQ	A155
ADBn	A70	CMPA	A157	ERSXn	A156
ADE	A116	CMPAQ	A159	ERXn	A153
ADL	A84	CMPQ	A158		
ADLA	A78	CMPXn	A160	FAD	A112
ADLAQ	A80	CNAA	A169	FCMG	A132
ADLQ	A79	CNAAQ	A171	FCMP	A131
ADLXn	A81	CNAQ	A170	FDI	A126
ADQ	A72	CNAXn	A172	FDV	A125
ADXn	A74	CWL	A161	FLD	A106
ALR	A67			FMP	A121
ASL	A61	DFAD	A114	FNEG	A129
ANA	A136	DFCMG	A134	FNO	A130
ANAAQ	A138	DFCMP	A133	FSB	A117
ANQ	A137	DFDI	A128	FST	A109
ANSA	A140	DFDV	A127	FSZN	A135
ANSQ	A141	DFLD	A107		
ANSXn	A142	DFMP	A123	GTB	A196
ANXn	A139	DFSB	A119	LACL	A230
AOS	A85	DFST	A110	LBRn	A13
ARL	A64	DIS	A198	LCA	A25
ARS	A58	DIV	A101	LCAQ	A27
ASA	A75	DRL	A199	LCQ	A26
ASQ	A76	DUFA	A115	LCXn	A28
ASZn	A77	DUFM	A124	LDA	A17
AWCA	A82	DUFS	A120	LDAQ	A19
AWCQ	A83	DVF	A102	LDB	A14
				LDBR	A15
BCD	A195	EAA	A8	LDCF	A16
		EABn	A11	LDE	A108
CAM	A194	EAPn	A12	LDI	A23
CANA	A165	EAQ	A9	LDQ	A18
CANAAQ	A167	EAXn	A10	LDT	A20
CANQ	A166	ERA	A150	LDXn	A21
CANXn	A168	ERAQ	A152	LLR	A69
CIOC	A197	ERQ	A151	LLS	A63

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Spec. No. M50EB00107
Cont. on Sh.A243 Sh. No. A242

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

<u>MNEMONIC</u>	<u>Page</u>	<u>MNEMONIC</u>	<u>Page</u>	<u>MNEMONIC</u>	<u>Page</u>
LREG	A24	SAM	A29	SWCA	A97
LRL	A66	SBA	A86	SWCQ	A98
LRS	A60	SBAQ	A88	SXLn	A41
LXLn	A22	SBLA	A93	SZN	A163
		SBLAQ	A95		
MME	A201	SBLQ	A94	TEO	A191
MME2	A203	SBLXn	A96	TEU	A192
MME3	A205	SBQ	A87	TMI	A186
MME4	A207	SBRn	A31	TNC	A189
MPF	A200	SBXn	A89	TNZ	A185
MPY	A99	SCU	A49	TOV	A190
		SDBR	A33	TPL	A187
NEG	A104	SMCM	A213	TRA	A173
NEGL	A105	SMIC	A215	TRC	A188
NOP	A229	SREG	A42	TSBn	A174
		SSA	A90	TSS	A177
ORA	A143	SSQ	A91	TSXn	A176
ORAQ	A145	SSXn	A92	TTF	A193
ORSA	A147	STA	A36	TZE	A184
ORSQ	A148	STAC	A37		
ORSXn	A149	STAQ	A39	UFA	A213
ORXn	A146	STB	A32	UFM	A122
		STBA	A45	UFS	A118
PRQ	A144	STBQ	A46		
		STC1	A55	XEC	A209
QLR	A68	STC2	A56	XED	A210
QLS	A62	STCA	A43		
QRL	A65	STCD	A35	ZAM	A30
QRS	A59	STCQ	A44		
		STE	A111		
RCCL	A231	STI	A47		
RCU	A180	STPn	A34		
RET	A178	STQ	A38		
RMCM	A211	STT	A48		
RPD	A220	STXn	A40		
RPL	A224	STZ	A57		
RPT	A216				
RTCD	A179				
RSW	A228				

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Spec. No. M50EB00107

Cont. on Sh. F7-0 Sh. No. A243

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

RELEASES AND APPROVALS For: Sections 1-6 and Appendix A.

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Cont. on Sh. 7-1 Sh. No. 7-0

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

INTRODUCTION

Part II of this Engineering Product Specification (EPS) is essentially a detailed description of the GE-645 Prototype Processor hardware, both physically and electrically. After Section 7.0 which describes the physical configuration of the Processor, the theory of operation for the Processor and the individual functional units that make it up are explained, then the detailed operation.

EPS-I for the GE-645 Prototype Processor must be familiar to the reader before attempting to read EPS-II, since the material presented in the following pages is but a logical explanation of the philosophy stated in EPS-I.

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Spec. No. M50EB00107

Cont. on Sh. 8-1 Sh. No. 7-1

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

7.0 PHYSICAL CONFIGURATION

The GE-645 Prototype Processor is contained in a single double size cabinet (freestanding or one wing of a X or Y configuration). One end of the cabinet (G.E. Dwg. 43E160145) mounts the Maintenance Panel which is exposed to the operator. At the rear of the Maintenance Panel are the processor fault vector switches and memory interface controls. A complete description of the Maintenance Panel is given in Part I Section 3.0 of EPS-I. The opposite end of the Processor cabinet provides jack connectors (snowplow) for up to eight possible memory controllers, an elapsed time meter, power supplies for relay power, the primary input power circuit breaker, and a relay panel. This panel mounts the relays which select combinations of the approximately 1500 sampling points that are displayed on the Maintenance Panel indicators. All power supplies for the six frames of circuit cards are located in the center of the cabinet and behind the Maintenance Panel. The supplies for the Maintenance Panel display lamps are also mounted on brackets behind the Maintenance Panel. Voltage regulation dropping resistors for the various power supplies are mounted on the top of the cabinet.

The general layout of the Processor cabinet is given in paragraph 1.5 of EPS-I. For a more detailed explanation of the physical layout, refer to the cabinet mechanical drawings referenced from the top assembly drawing and P.L., 43E160145.

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Cont. on Sh. 9-1 Sh. No.8-1

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

8.0 OPERATIONAL DESCRIPTION

(To be supplied at a later date and will contain a top level discussion of total Processor operation: Operations Unit operations (loads, stores, etc.) Control Unit operations (special instructions, transfers, etc.) and how the Base and Interface Frames and associative memory are utilized to fetch instructions and operands. For the present, the only top level discussions are in EPS-I, Sections 1 and 2 and are not adequate for a general picture of the entire Processor.)

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PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh.9-2 Sh. No.9-1

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

9.0 CONTROL UNIT DETAILED THEORY

This section covers the detailed theory of operation of the Control Unit. The Control Unit consists of one frame of logic boards in the Processor cabinet designated the Control Frame. For the purpose of this discussion the names Control Unit and Control Frame are used interchangeably. The information in this section covers a brief general description of the Control Frame; the modes of operation generalized into classes of instruction that cause the same operating sequence; the principle hardware elements and functions; and the basic operating sequences that take place to perform the functions.

9.1 GENERAL DESCRIPTION

The major functions of the Control Frame are:

To perform all Processor control functions

To perform address modification when specified by the instruction or indirect word.

To define Processor mode of operation (Master/Slave, Absolute/Append)

To perform external interrupt recognition and servicing (including faults)

To perform operation decoding

To buffer a total of four instructions in the Processor at one time

Operation code buffering for two additional instructions that have the operand addresses prepared and are waiting to be accepted by the Operations Unit

At the present time, the meaning of the aforementioned major functions may appear vague, but the following paragraphs will elaborate all the functions in greater detail.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-3 Sh. No. 9-2

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.1 - contd

To perform the basic functions listed above requires almost a full complement of component boards in the Control Frame. Since most of the control frame logic deals with control functions, the block diagram (43D160212) and the control diagrams (43D163387) cannot show neatly defined packages of logic that perform well defined functions. Therefore, the discussion in the following paragraphs is presented in this manner:

- 1) Modes and sequences of operation within the Control Frame are grouped according to the similarity of the sequences involved in executing the specific instruction beginning in paragraph 9.2. Modes and sequences of operation that cannot be generalized, are explained in detail.
- 2) The principle hardware elements and functions that can be defined physically or functionally are explained in detail beginning in paragraph 9.3.
- 3) The interrelationship of the various functions and hardware elements, and how they perform the basic functions in each mode and sequence of operation, is covered in detail beginning in paragraph 9.4.

Presumably the reader will be able to supply the finer details of the logical operation by reference to the applicable logic prints and diagrams referenced during the following discussions.

9.1.1 INTERFACE LINE SUMMARY

All interface signals between the Control Frame and other frames within the Processor are listed by EDA mnemonic in Tables 9.1.1 and 9.1.1a. The total interface between all frames in the Processor is listed in drawing 43A164138.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.9-4 Sh. No.9-3

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE 9.1.1 Control Frame Inputs

Mnemonic	Description
<u>Arithmetic Frame</u>	
DFNRC (FNR)	FLAG TO CF-OU READY FOR DIRECT OPERAND
DFNYC (FNY)	FLAG TO CF-M REG. RDY FOR OPERAND
DRGSC	GS BUT NOT GF
DRIJC	A TERMINATE REPEAT MODE CONDITION HAS OCCURRED
DTASC	TEST AND STEP
EN18C-EN35C	SCANNER LOGIC
FE00C-FE07C (EO-7)	8-BIT EXPONENT REGISTER
FI00C-FI09C (IND0-9)	INDICATOR REGISTER
QSLTC (\$LAST)	
QZGGC	GENERAL STROBE
QZZAC (\$DVCK)	DIVIDE CHECK FAULT PULSE
QZZOC (\$FOLF)	OVERFLOW FAULT PULSE
<u>Register Frame</u>	
DDACD	XFER CNTRL. FOR E REG. 0-7 TO ZDO 0-7
F000D-F017D (X0 0-17)	18-BIT INDEX REGISTER NO. 0
F100D-F117D (X1 0-17)	18-BIT INDEX REGISTER NO. 1
F200D-F217D (X2 0-17)	18-BIT INDEX REGISTER NO. 2
F300D-F317D (X3 0-17)	18-BIT INDEX REGISTER NO. 3
F400D-F417D (X4 0-17)	18-BIT INDEX REGISTER NO. 4
F500D-F517D (X5 0-17)	18-BIT INDEX REGISTER NO. 5
F600D-F617D (X6 0-17)	18-BIT INDEX REGISTER NO. 6
F700D-F717D (X7 0-17)	18-BIT INDEX REGISTER NO. 7
FA00D-FA71D (AQ 0-71)	72-BIT AQ REGISTER (0-35 A)(36-71 Q)
FDPFD	INDICATES LWR. 36 BITS DBL. P. OPRND. NEXT ON ZDI

COMPANY CONFIDENTIAL
 GENERAL ELECTRIC COMPANY
 COMPUTER EQUIPMENT DEPARTMENT
 PHOENIX, ARIZONA

Spec. No. M50EB00107
 Cont. on Sh.9-5 Sh. No.9-4

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

TABLE 9.1.1 Control Frame Inputs (contd)

Mnemonic	Description
	<u>Register Frame</u>
FM28D	MEMORY OPERAND BIT 28-APPENDING MODE
QZQBD (\$QR)	O-REGISTER STROBE
QZSSD (\$START)	START STROBE
QZSZD (\$SDY)	OU STORE DATA READY TO STORE
QZYXD (\$YRY)	OU READ FOR NEW OP CODE
	<u>Base Frame</u>
BCLTF ($\overline{\text{FLT}}$)	RECOGNIZE FAULT TAG 1-3
BEOTF ($\overline{\text{BIT 29+ITS+ITB}}$)	
BFRQF ($\overline{\text{FRQ}}$)	GROUP 6 FAULT PRESENT
BLPCF	LOW PRIOR. FLTS/\$ABT
BONCF (GP2 PONC)	GP2 AND PONC
BPETF (PBR=TBR)	CONTENTS OF PBR EQUALS TBR CONTENTS
BRROF ($\overline{\text{RR}}$)	RELEASE \$R
BS03F (RS3)	RESET GROUP 3,4,5,6 FAULTS
BSBTF (SABT)	START ABORT SEQUENCE
BSFFF ($\overline{\text{SFF}}$)	STOP FOR FAULTS
DFAOF-DFA4F (FAA-E)	FAULT ADDRESS ENCODES (FAO MOST SIG.)
DI00F-DI35F (ZDIO-35)	DATA INPUT BUS
DOMRF	MEMORY READY
DZ00F-DZ17F (ZBRI0-17)	BASE REGISTER INTERNAL BUS
EDPIF (DPI)	DOUBLE PI CYCLE
EFOCF (FOC)	FAULTY OP. CODE FAULT
EGBOF (GBO)	GENERAL BASE INSTRUCTION F/F
EINAF	INITIALIZE
EN03F-EN05F (INC3-5)	INCREMENTOR REGISTER

COMPANY CONFIDENTIAL
 GENERAL ELECTRIC COMPANY
 COMPUTER EQUIPMENT DEPARTMENT
 PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.9-6 Sh. No. 9-5

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

TABLE 9.1.1 Control Frame Inputs (contd)

Mnemonic	Description
	<u>Base Frame</u>
EPEOF ($\overline{PEO}$)	PARITY ERROR IN OPERAND
EPFIF ($\overline{PFPI}$)	PARITY ERROR IN BUFFRD. INSTRCN.
ERSTF	REMOTE STOP F/F
ESEPF (SEP)	PRTY, ERR. IN OU OPERAND
ESNOF (SNO)	SNAPSHOT ZERO F/F
ESN1F (SN1)	SNAPSHOT ONE F/F
EWCCF ($\overline{WC}$)	WAIT FOR EXECUTE INTRPT. CELL NO. CYCLE
EWFOF (WF)	ABORT F/F
EWFBF (WFTB)	WAIT FOR TROUBLE FLIP-FLOP
QABTF (\$ABT)	END OF WF PULSE
QSBTF	START ABORT PULSE
QSNOF (\$SNO)	END OF SNAPSHOT 0 PULSE
QSNZF (\$SN1)	END OF SNAPSHOT 1 PULSE
QZBCF (\$BC)	DATA IS READY
	<u>Interface Frame</u>
BDPCM	SET DPIN F/F
BFAAM ($\overline{FA}$)	FINAL ADDRESS FETCH (FAPM+FANP+ABS)
BIAOM-BIA3M (IBA0-3)	INTERRUPT BLOCK ADDRESS BITS 0-3
BLSRM	INT BLOCK ADDRESS BIT
BSCAM	DELAYED TRIGGER
BSCHM	SCOPE GATE
DAIPM-DHIPM ($\overline{IPO-7}$)	EXTERNAL INTERRUPT PRESENT-PORTS A-H
EMS2M (MSF2)	NEXT INST. PR. MASTER/SLAVE MODE BUFFER
EMLSM	MULT. LOAD/STORE INSIGN. FLAG
ERDYM (SRDY)	PROC. READY FOR STEP FLAG

COMPANY CONFIDENTIAL
 GENERAL ELECTRIC COMPANY
 COMPUTER EQUIPMENT DEPARTMENT
 PHOENIX, ARIZONA

Spec. No. M50EB00107
 Cont. on Sh.9-7 Sh. No.9-6

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

TABLE 9.1.1 Control Frame Inputs (contd)

Mnemonic	Description
	<u>Interface Frame</u>
FNOOM-FN17M (SCA0-17)	SCANNER BITS 0-17
MA15M-MA17M (RS15-17)	RS-ADDER BITS 15-17
QDSTM (\$DS)	DATA STORED PULSE
QIAZM (\$IAZ)	
QIFFM (\$IFF)	INTERFACE FRAME FINISHED PULSE
QINTM (\$INT)	GENERAL \$INT
QOPNM (\$PIN)	
QPRIM (\$PRI)	
QSDAM (\$DA)	
QSRFM (\$RSRF)	APPNDG. FETCH STARTED PULSE
QSSFMM (\$SSRF)	FINAL FETCH STARTED PULSE
	<u>Maintenance Panel</u>
SASMT	ASSOC. MEMORY OFF SWITCH
SCOOT	OU/CU OLAP OFF SWITCH
SI00T-SI35T	36-BIT INSTRUCTION WORD SWITCHES
SQC1T	CU TEST CLOCK SWITCH
SREXT	REPEAT EXECUTE SWITCH
SSMT	STEP MEMORY SWITCH
SSOFT	OFF SWITCH
SSOPT	STOP SWITCH
SSPGT	STEP PROGRAM SWITCH
STMRT	REAL-TIME/MEM. CYCLE SWITCH FOR TIMER REGISTER
SSTPT	STEP SWITCH
STSTT (TEST)	TEST SWITCH
SXECT	EXECUTE BUTTON
SXSWT	EXECUTE SWITCHES

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-8 Sh. No. 9-7

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE 9.1.1a Control Frame Outputs

Mnemonic	Description
	<u>Arithmetic Frame</u>
BRDRB ($\overline{\text{RDR}}$)	REPEAT DOUBLE RETURN
BRLRB ($\overline{\text{INT}}$)	REPEAT OR LINK RETURN
BRSTB ($\overline{\text{RST}}$)	RETURN SENSE TERMINATION
DFCTB (TALLY)	
DTHAB (FL) (PA)	PREP. ADDRESS BUT NOT REPEAT LINK
DTHCB ($\overline{\text{CRESET OVFL}}$)	RESET OVERFLOW
DTHDB ($\overline{\text{CRESET EOFL}}$)	RESET EXPONENT OVERFLOW
DTHEB ($\overline{\text{CRESET EUFL}}$)	RESET EXPONENT UNDERFLOW
DYSZB (YS=0)	Y-ADDER OUTPUT IS ZERO
DZ06B-DZ17B	INSTRUCTION DECODE TO ADDRESS ADDER
EI10B	MASTER MODE INDICATOR
EPAFB	PREPARE FIRST ADDRESS CYCLE
EPIFB	PREPARE INST. ADDRESS
EPNFB	REPEAT MODE INDIRECT CONTROL
EPRFB	PREPARE REWRITE CYCLE FLAG
EPTFB	PREPARE IT ADDRESS
EPZFB	PREPARE SUBSEQUENT ADDRESS CYCLE AFTER PA INDIRECT
QZRAB (\$RESET ABORT)	RESET ABORT STROBE
QZSAB (\$SET ABORT)	SET ABORT STROBE
	<u>Register Frame</u>
DC00B-DC08B ($\overline{\text{ZORO-8}}$)	OPER. TRANSMIT BUS TO OU
DDAMB ($\overline{\text{PR}}$)	CONTROL FRAME IN PR CYCLE
DTHUB ($\overline{\text{FD+FT+FL}}$)	ANY REPEAT INSTRUCTION (FT+FD+FL)
DW12B (ZI12)	BYTE SIZE BIT
DW15B-DW17B ($\overline{\text{ZI15-17}}$)	BYTE POSITION BITS
EI10B ABS	MASTER MODE INDICATOR

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.9-9 Sh. No.9-8

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE 9.1.1a Control Frame Outputs (contd)

Mnemonic	Description
	<u>Register Frame</u>
ELOOB-EL17B (ICTA0-17)	ADDRESS OF INST. IN EXECUTION
MU00B-MU17B (YS0-17)	ADDRESS ADDER
QRDYB (\$DRDY)	DATA READY TO RF STROBE
QZOYB (\$ORY)	OP CODE IS READY STROBE
QZPOB (\$64 KC)	64-KC STROBE
QZPQB (\$BYTE)	BYTE POSITION REGISTER STROBE
QZPXB (\$X0-7)	INDEX REGISTERS STROBE
	<u>Associative Memory Frame</u>
MBOOB-MB11B (BS0-11)	ADDRESS BASE ADDER
QSTAB (\$)	START ASSOC. MEMORY PULSE
QDMFB	STROBE DIRECT OPERAND
QESRB	PREPARE INTERRUPT STROBE
QSCAB	STROBE TO SCANNER LOGIC
	<u>Base Frame</u>
BBCRB (BCR)	INSTRUCTION IS REPEAT OR STORE
BCDBB (CDB0-17/)	CONTROL FOR DB-REG./ZDIBF0-17
BCTAB (CT)	TAG REG. MODIFICATION IDC OR DIC
BDDBB (CDB0-17/)	CONTROL FOR DB-REG./ZDIRF18-35
BDPIB (SPI)	DECODE=SPI=DPI AND EXI AND RPI
BEADB (EA)	PREPARED ADDRESS IS FOR OPERAND
BHLTB (HALT)	LOGIC DECODE FOR STOP
BICFB (CSETIC)	LEVEL TO SET IC FLIP-FLOPS
BICRB (CRESET IC)	LEVEL TO RESET IC FLIP-FLOPS
BIPCB ($\overline{PC}$)	INTERRUPT PRIORITY CHANNEL
BIPFB ($\overline{IPF}$)	DECODE LOGIC IPR STROBE
BMPAB (FRA)	FAULT OR EXECUTE INT. IN PA CYCLE
BPNLB (CPNL SW/ZDI)	CONTROL FOR PANEL SWITCHES/ZDIRFO-35

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-10 Sh. No. 9-9

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE 9.1.1a Control Frame Outputs (contd)

Mnemonic	Description
	<u>Base Frame</u>
BSPAB (CSET PA)	LEVEL TO SET PA FLIP-FLOP
BSPIB (CSET PI)	LEVEL TO SET PI FLIP-FLOP
BSPNB (CSET PN)	LEVEL TO SET PN FLIP-FLOP
BSPTB (CSET PT)	LEVEL TO SET PT FLIP-FLOP
BSPZB (CSET PZ)	LEVEL TO SET PZ FLIP-FLOP
BSWNB (CSET WN)	LEVEL TO SET WN FLIP-FLOP
BTDLB (TMCH=2)	TOO MUCH COUNTER EQUALS 2
BTDMB (TMCH=1)	TOO MUCH COUNTER EQUALS 1
BTDNB (TMCH=0)	TOO MUCH COUNTER EQUALS 0
BTRGB (TRG01)	TRANSFER GO GROUP SUB11 DECODE
BYCFB (Y)	DIRECT OPERAND THE Y OF IT
DZERB (CZEROES/)	CONTROL FOR ZEROS/ZDIRFO-17
DA00B-DA02B (ZY0-2)	INST. REG. SW. EVEN
DA29B (ZY29)	INST. REG. SW. EVEN
DB00B-DB02B (ZC0-2)	INST. REG. SW. ODD
DB29B (ZC29)	INST. REG. SW. ODD
DW00B-DW08B (ZIO-8)	INST. REGISTER DECODE BUS
DW12B-DW17B (ZI12-17)	INSTRUCTION REGISTER DECODE BUS
ECICB (CIOC)	FF HOLDING INTERFACE TERM WHEN CIOC INST. GIVEN.
EDVKB (DVCK)	DIVIDE CHECK FF
EEXFB (EXF)	EXECUTE FF
EFLFB (FOLF)	FAULT OVERFLOW FF
EKC1B (1KC)	TIMER 1KC OUTPUT
ELSTB (LST1)	
EMSYB (M/S)	MASTER/SLAVE FLAG ICTA8
ERPDB (FD)	REPEAT DOUBLE MODE

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-11 Sh. No.9-10

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE 9.1.1a Control Frame Outputs (contd)

Mnemonic	Description
	<u>Base Frame</u>
ERPLB (FL)	REPEAT LINK MODE
ESPRB	CONTROL FRAME STEP FLAG
ERPTB (FT)	REPEAT MODE
ESTPB (STOP)	STOP FLIP-FLOP
ETERB (TERM)	TERMINATION OF INSTRUCTION
EWIWB (WI2)	WAIT FOR INST. FOR I-REG.
EXDEB (XDE)	EXECUTE DOUBLE FROM EVEN LOCATION
MBOOB-MB17B (BS0-17)	ADDRESS BASE ADDER
QIPRB (\$IPR)	STROBE TO SET IPR FLIP-FLOPS
QSCOB (\$C)	\$C TO BASE FRAME
QZCEB	STROBE EVEN SEG TAG REG
QZCOB	STROBE ODD SEG TAG REG
QZCRB (\$CSR)	\$CSR TO BASE FRAME
QZSRB (\$R)	GENERAL STROBE IN CF
	<u>Interface Frame</u>
BEADB (EA)	PREPARED ADDRESS IS FOR OPERAND
BFSLB (RPTS)	REPEAT FLAG DECODE FD, FT, OR FL
BIPCB (PC)	INTERRUPT PRESENT
BISIB	INHIBIT START INTERRUPT
BMPAB (FPA)	FAULT OR EXECUTE INT. IN PA CYCLE
BSITB	STOP FOR TERMINATE
BSPAB (CSET PA)	LEVEL TO SET PA
BSPIB (CSET PI)	LEVEL TO SET PI FF
BSPNB (CSET PN)	LEVEL TO SET PN
BSPRB (CSET PR)	LEVEL TO SET PR FF
BSPTB (CSET PT)	LEVEL TO SET PT

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-12 Sh. No. 9-11

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE 9.1.1a Control Frame Outputs (contd)

Mnemonic	Description
	<u>Interface Frame</u>
BSWNB (CSETWN)	LEVEL TO SET WN FF
BTBCB	STOP OR FAULT TO SYNC PANEL
BTRGB (TRG01)	TRANSFER GO GROUP SUB 1 DECODE
BYCFB	DIRECT OPERAND
DD00B-DD35B (ZEOCF0-35)	CONTROL FRAME DATA OUTPUT BUS
DW00B-DW17B (ZIO-17)	INST. REG. DECODE BUS
ECTO B-ECT5B (CT0-5)	TAG BIT STORAGE REGISTER
ECICB	INTERFACE TERM FOR CIOC INST.
EMSYB (MSY)	MASTER/SLAVE FLAG ICTA8
ERPOB-EPR7B (IPRO-7)	INTERRUPT PRIORITY REGISTER
EXSFB (XSF)	EXECUTE SWITCHES FAULT
MBOOB-MB17B (BS0-17)	ADDRESS BASE ADDER
QAAMB (\$AAM)	START ASSOCIATIVE APPENDING STROBE
QCFFB (\$CFF)	COMPARE STROBE
QPRCB (\$PRC)	STROBE R GEN CONTROLS
QSABB (\$SAB)	START ABSOLUTE STROBE
QSAPB (\$SAP)	START APPENDING STROBE
QSCAB (\$SCA)	STROBE TO SCANNER LOGIC
SZCCB (\$C)	GENERAL STROBE
QZDPB (\$DP)	CF DATA AVAILABLE STROBE
<u>Relay Box</u>	
EC00B-EC08B (C00-8)	OPERAND DECODE-ODD
ECTO B-ECT5B (CT0-5)	TAG BIT STORAGE REGISTER
EHOOB-EH11B	ICTA PRIME REG
EJOOB-EJ17B (ICTC0-17)	18-BIT Y AND C PAIR ADDRESS INSTRU- TION COUNTER

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.9-13 Sh. No.9-12

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE 9.1.1a Control Frame Outputs (contd)

Mnemonic	Description
	<u>Relay Box</u>
ED00B-EK17B (ICTB0-17)	18-BIT I-BUFFER CONTENTS ADDRESS CONTENTS ADDRESS INST. COUNTER
EL00B-EL17B (ICTA0-17)	18-BIT EXECTN. INSTR. ADDRESS INSTR. COUNTER
EZ10B-EX13B (Z1 0-3)	Z-FUNCTION REGISTER NO. 1
EZ20B-EZ23B (Z2 0-3)	Z-FUNCTION REGISTER NO. 2
FC00B-FC35B (C0-35)	36-BIT INSTRUCTION DECODE REGISTER- ODD
FCE0B-FCE8B (CE0-8)	OPERAND DECODE-EVEN
FI00B-FI71B (ID-71)	72-BIT INSTRUCTION REGISTER
FY00B-FY35B (Y0-35)	36-BIT INSTRUCTION DECODE REGISTER- ODD
MB00B-MB17B (BS0-17)	ADDRESS BASE ADDER
MU00B-MU17B (YS0-17)	18-BIT ADDRESS ADDER
	<u>Maintenance Panel</u>
BHL2B (HALT2)	HALT TO CONTROL PANEL
BIPCB (PC)	INTERRUPT PRIORITY CHANNEL
BJR2B	DECODE FOR TRG02
EBFRB (BFR)	CONTROL FF IN STROBE R GENERATION
ECFRB (CFR)	CONTROL FF FOR STROBE R GENERATION DELAY
EI10B (ABS)	MASTER MODE INDICATOR
EICFB (IC)	XFER DATA TO ZI BUS FF
EIFRB (IFR)	CONTROL FF FOR STROBE R GENERATION
EMF0B (MF0)	MFREE COUNTER
EMF1B (MF1)	MFREE COUNTER
EMSIB (MSI)	MASTER/SLAVE FLAG SUB 2 IN CONTROL FRAME
EMSYB (MSY)	MASTER/SLAVE FLAG ICTA8

COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-14 Sh. No. 9-13

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

TABLE 9.1.1a Control Frame Outputs (contd)

Mnemonic	Description
<u>Maintenance Panel</u>	
EPAFB (PA)	PREPARE FIRST ADDRESS CYCLE
IPIFB (PI)	PREPARE INSTRUCTION ADDRESS
IPINB (PIN)	FF IN BINTB DECODE
EPNFB (PN)	REPEAT MODE INDIRECT CONTROL
EPTFB (PT)	PREPARE IT ADDRESS
EPZFB (PZ)	PREPARE NEXT ADDRESS CYCLE AFTER PA IN INDIRECT
ESDYB (SDY)	FF IN BINTB DECODE
ESREB (SRF3)	SRF3 F/F
ESREB (SRF2)	SRF2 F/F
ETJSB (B)	XFER DATA TO ZOR BUS S FF
ETMOB-ETM2B (TMCH0-2)	TOO MUCH COUNTER 0-2
EXDEB (XDE)	EXECUTE DOUBLE FROM EVEN LOCATION
EXDOB (XDO)	EXECUTE DOUBLE FROM ODD LOCATION
<u>Junction Panel</u>	
B999B (MEM. READYC)	MEMORY READY TO CONSOLE
BCPOB	ABSOLUTE MODE TO CONSOLE
BTNLB (START UP)	PROC. READY TO CONSOLE
BWHOB	WAIT FOR INTERRUPT TO CONSOLE
QEARB	PULSE TO CONTROL SPEEDMETER

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2 MODES AND SEQUENCES OF OPERATION

The modes and sequences of operation within the Control Frame are divided into the following general categories:

- 1) Mode of Addressing - whether the Processor is in the Absolute or Append mode of addressing for instructions and operands, and what operand address modification is employed.
- 2) Mode of Execution - whether the Processor is executing instructions in the Master or Slave mode.

In preparing the addresses for instructions and operands, and in the execution of these instructions, the Control Frame goes through a certain sequence of operation. For the purpose of explanation, the sequences have been defined as follows:

- 1) Instruction fetches - for two or four instructions.
- 2) Operand fetches - generally dependent on the type of instruction to be executed:
 - a) Normal Operations Unit (OU) -- those OU instructions which require an operand to be fetched from, or sent to memory.
 - b) Direct Operations Unit -- those OU instructions that do not require a memory access for the operand.
 - c) Control Frame (CF) -- those instructions which are executed primarily within the Control Frame.
 - d) Base Frame (BF) -- those instructions which involve the Base and/or Associative Memory Frames and generally are executed outside the Control Frame.
 - e) Specials -- those instructions which involve multiple frames and individually determine the Control Frame sequence.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-16 Sh. No. 9-15

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2 - contd

The sequence of operation is determined by a series of sequence control flags that are set as a function of the decoded instruction, and by the previous and the succeeding sequences.

9.2.1 SEQUENCE CONTROL FLAGS

The timing sequences of the Control Frames are defined by flip-flops called flags. There are four general categories of flags:

- 1) Prepare
- 2) Wait for memory
- 3) Even/odd sequence
- 4) Auxiliary or special

9.2.1.1 Prepare (P) Flags

The prepare flags are used to define the prepare sequence for instruction, operand, indirect, and indirect then tally word address preparation. These flags are defined as follows:

- 1) PI - Prepare Instruction (flip-flop). This flag defines with a few exceptions, that period of time that an address for a double-precision instruction fetch is prepared. The PI flag is normally set whenever instructions are to be loaded into the I-register.
- 2) PA - Prepare Address (flip-flop). This flag defines that period of time during which the preparation of an address for an or the first indirect word specified by the instruction word is accomplished.
- 3) PZ - Prepare Address of Indirect (flip-flop). This flag defines that period of time during which an operand address is prepared using an indirect word that was pulled from memory as the result of RI or IR modification in the instruction word, (that is, any PA cycle but the first).
- 4) PN - Prepare Repeat Indirect (flip-flop) defines that period of time used to prepare the operand address from an indirect word "repeated" instructions having

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-17 Sh. No. 9-16

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.1.1 - contd

RI modification, and for preparing the transfer address of a return or return double instruction.

- 5) PT - Prepare IT Operand (flip-flop) defines that period of time during which the preparation of an address using an indirect word brought in as a result of IT modification is accomplished.
- 6) PR - Prepare Rewrite (flip-flop) defines that period of time during which the address and tally portions of an indirect word brought in as a result of IT modification is updated, and the new updated indirect word is returned to memory for storage.
- 7) PC - Prepare Execute Interrupt (level) defines that period of time during which an XEC memory command is prepared to acknowledge the presence of an external interrupt. All prepare flags are mutually exclusive except that PC may be set during the first 300 nanoseconds of PA, PZ, PN or PT. The prepare flags are set as a function of strobe \$C and the particular prepare operation being performed. Strobe \$C in turn is a function of any conditions which are discussed in detail under strobe generation, paragraph 9.3.1.

9.2.1.2 Wait for Memory (W) Flags

The wait for memory flags are used to define the particular wait for memory cycles as follows:

- 1) W- Wait for Operand (flip-flop) defines that period of time that the Processor is waiting for an operand from memory, or memory is to accept an operand from the Processor.
- 2) WI₁ - Wait for Instruction 1 (flip-flop) defines that period of time that the Processor is waiting for the memory to send it an even instruction, an odd instruction or an even/odd pair of instructions for the Y- and C-registers.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.1.2 - contd

- 3) WI₂ - Wait for Instruction 2 (flip-flop) defines that period of time that the Processor is waiting for an even/odd pair of instructions to fill the I-register.
- 4) WC - Wait for Execute (flip-flop) defines that period of time during which the Processor is waiting for the memory to acknowledge an Execute command which was issued in response to an external interrupt. This flag is located in the Processor fault logic in the Base Frame but is included here since it defines a Control Frame sequence.
- 5) WF - Wait for Fault (flip-flop) defines that period of time after the presence of a fault has been established, during which the proper conditions are established for entrance into a fault routine. The WF flag is located in the processor fault logic in the Base Frame but is included here since it defines a particular Control Frame sequence.
- 6) WN - Wait for Indirect (flip-flop) defines the period of time during which the Processor is waiting for an indirect word from Memory.

Flags WI₁, WI₂ and WC are mutually exclusive with each other and with all P flags except that PA may overlap WI₂. The W flag will be on in parallel with a P or a different wait flag, if an Operations Unit operand is being fetched from memory.

9.2.1.3 Even/Odd Sequence Flag

A flag denoted as the IC flip-flop is used to designate whether the Control Frame is working on the even (Y) or odd (C) instruction register. The IC flip-flop is reset for the even instruction and set for the odd instruction. Reset and set conditions are a function of the strobe SC that initiates the beginning of the PA cycle for each instruction.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.9-19 Sh. No.9-18

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.1.4 Auxiliary or Special Flags

Within the Control Frame are a number of flags that define unique conditions that effect the operating sequence, or define a particular condition of an operating sequence. For instance:

- 1) FT - Repeat (flip-flop) when set denotes that the next instruction is to be repeated until prespecified terminate conditions have been met.
- 2) FD - Repeat Double (flip-flop) when set denotes that the next even/odd pair of instructions are to be repeated until prespecified terminate conditions have been met.
- 3) FL - Repeat Link (flip-flop) when set denotes that the next instruction is to be repeated using an operand link address contained within the data fetched from memory. The instruction will be repeated until a prespecified terminate condition has been met or until a "link address" of zero has been found.
- 4) RF - Repeat First (flip-flop) when set defines the first time that an effective address for an operand is prepared when in a Repeat, Repeat Double (first time for the pair of the repeated instructions), or Repeat Link mode of operation.
- 5) TRMF - Terminate Repeat (flip-flop) is set upon detection of a Repeat mode terminate condition. It enables the Control Frame to enter a Terminate mode of operation designated TERM. TERM and the repeat flags are reset at end of the current prepare cycle (PA if no indirects, PN if indirects).
- 6) XDE - Execute Double Even (flip-flop) is set if an execute double instruction occurs as an even instruction or if IC is reset when an execute double instruction is forced into the Y- and C-registers (for a fault or in response to an interrupt request).

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-20 Sh. No.9-19

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

9.2.1.4 - contd

- 7) XDO - Execute Double Odd (flip-flop) is set if an execute double instruction occurs as an odd instruction or if IC is set when an execute double instruction is forced into the Y- and C-registers (for a fault or in response to an interrupt request).
- 8) MSY - Master/Slave for Y (flip-flop) is set when instructions are loaded into the Y- and C-registers if the addressing mode is absolute or if the segment descriptor of the current procedure indicates Procedure-Master when the addressing mode is append. The descriptor of the current procedure is defined by bits 27-35 of the Segment Descriptor Word contained in the Descriptor Register of the Interface Frame. MSY is set whether the instructions to the Y- and C-registers are from the data-in bus (ZDI) or the I-register.
- 9) MSI - Master/Slave for I (flip-flop) is set whenever instructions are loaded into the I-register when the segment descriptor of the current procedure indicates Procedure-Master.
- 10) ABS - Absolute (flip-flop) when set indicates that addressing is to be done in the Absolute mode (refer to paragraph 2.3). When reset addressing is done in the Append mode except for fault and interrupt responses. This flip-flop corresponds to bit 28 in the indicator register.
- 11) MASF - Temporary Absolute (flip-flop) when set indicates that the Processor is addressing in the Absolute mode. This mode is entered when instruction pair that is "brute forced" as the result of a fault or interrupt (Processor is in a WF cycle and not stopped). The temporary absolute flip-flop may also be effected by an RCU instruction.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-21 Sh. No. 9-20

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.2 INSTRUCTION AND OPERAND ADDRESS MODES

As mentioned previously in paragraph 2.3, addressing in the GE-645 is done in either the Absolute or the Append mode as specified by the condition of the Absolute (ABS) flip-flop in the Control Frame. Addressing is normally done in the Append mode. In the Append mode the effective address in the BS-adder is appended with an address pointer from the Base Frame in the RS-adder of the Interface Frame to form a 18-bit address, which is then formulated into a 24-bit address for the core location.

When addressing for instructions in the Absolute mode, the effective address becomes the core location that is accessed. When addressing for operands in the Absolute mode however, the effective address may be appended to form a 24-bit address. This is possible if an address pointer is generated because bit 29 of the instruction word is a "1" or because an ITS or ITB modifier is received during any operand address preparation cycle. If appending is done for operands while in the Absolute mode, the state of the Absolute flip-flop is not effected, but a strobe which tells the Interface Frame to ignore any appending is inhibited.

The Absolute flip-flop is set by one of the following conditions.

- 1) Addressing is being done in a Temporary Absolute mode because of a fault or external interrupt condition and a satisfied transfer (other than a TSS), that does not involve generation of an address pointer for the transfer address is executed. An address pointer is generated if bit 29 of the transfer is a "1" or ITS or ITB modifier is involved in obtaining the transfer address.
- 2) A RTD, RET or RCU instruction fetched from a Procedure-Master segment, is executed and it causes bit 28 of the Indicator Register to set (this bit corresponds to the Absolute indicator).

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-22 Sh. No. 9-21

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.2 - contd

The Append mode is entered (absolute flip-flop is reset) via one of the following:

- 1) A RTD, RET or RCU instruction, fetched from a Procedure-Master segment is executed and it causes bit 28 of Indicator Register to reset.
- 2) A TSS instruction is executed.
- 3) A satisfied transfer that generates an address pointer is executed (bit 29 of the transfer is a "1" or an ITS or ITB modifier is encountered in obtaining the transfer address).

Temporary Absolute mode (MASF - flip-flop set) is entered when a fault condition has been detected and is about to be serviced (if the Processor is not stopped), or if an RCU restores it to the set state. During the temporary Absolute state, a "brute force" XED instruction is formulated and the fault vectors are executed. The Temporary Absolute mode is exited to either the Absolute or the Append mode (providing another fault does not occur in the XED) if one of the fault vectors contains:

- 1) An RCU instruction which restores it to the reset state.
- 2) A RTD or RET instruction or any satisfied transfer.

If neither of the above two conditions are met, MASF is reset when a PI cycle is entered after the XED is completed.

9.2.2.1 Operand Address Modification

With few exceptions, all instructions in the GE-645 instruction set provide for some form of address modification for the operand. The different types of address modification are described in paragraph 2.6.1. A flow chart of the different types of address modification is presented in Figure 9.2.2.1. This flow chart is rather general in nature but contains sufficient

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-23 Sh. No. 9-22

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.2.1 - contd

information to enable the reader to follow the address modification sequence in conjunction with the Control Frame block diagram, 43D160212 sheet 5. The detailed address modification sequences are covered in paragraph 9.4.

R (Register) Modification

With R modification (t_m of instruction word tag = 00) one of 13 registers are added to the instruction address (bits 0-17 of instruction contained in the Y- or C-register) in the YS-adder. If the register designator (t_d of instruction word) designates that bits 0-17 of the instruction word constitute a direct operand (DU, DL modification) then bits 0-17 of the instruction word are sent directly to the Register Frame of the Operations Unit via the BS-adder, and no memory access is required for the operand. However, if bit 29 of this instruction word is set, this indicates that bits 0-2 of the instruction word designate an address base register for address, appending and an internal base may be added to the address in the BS-adder before an operand is fetched. An R modification terminates any further address modification.

The operation code and tag portions (bits 18-35) of the instruction word are switched to the control point decode logic; the selection of the Y- or C-register for an instruction is determined by the reset or set condition of the IC flip-flop. For this discussion only the Y-register is considered (IC reset). Decoding of an R modifier in the t_m portion of the instruction word tag, allows the t_d portion to be switched to the ZX switch decode logic, via the ZI_{14-17} (ZI/ZT) switch, and select one of 13 registers for modification. The selected register is then added to the tentative operand address of the instruction word in the YS-adder. If t_d selects DU or DL modification, the operand address in the YS-adder is the operand. The output of the YS-adder is then present at the input to the BS-adder.

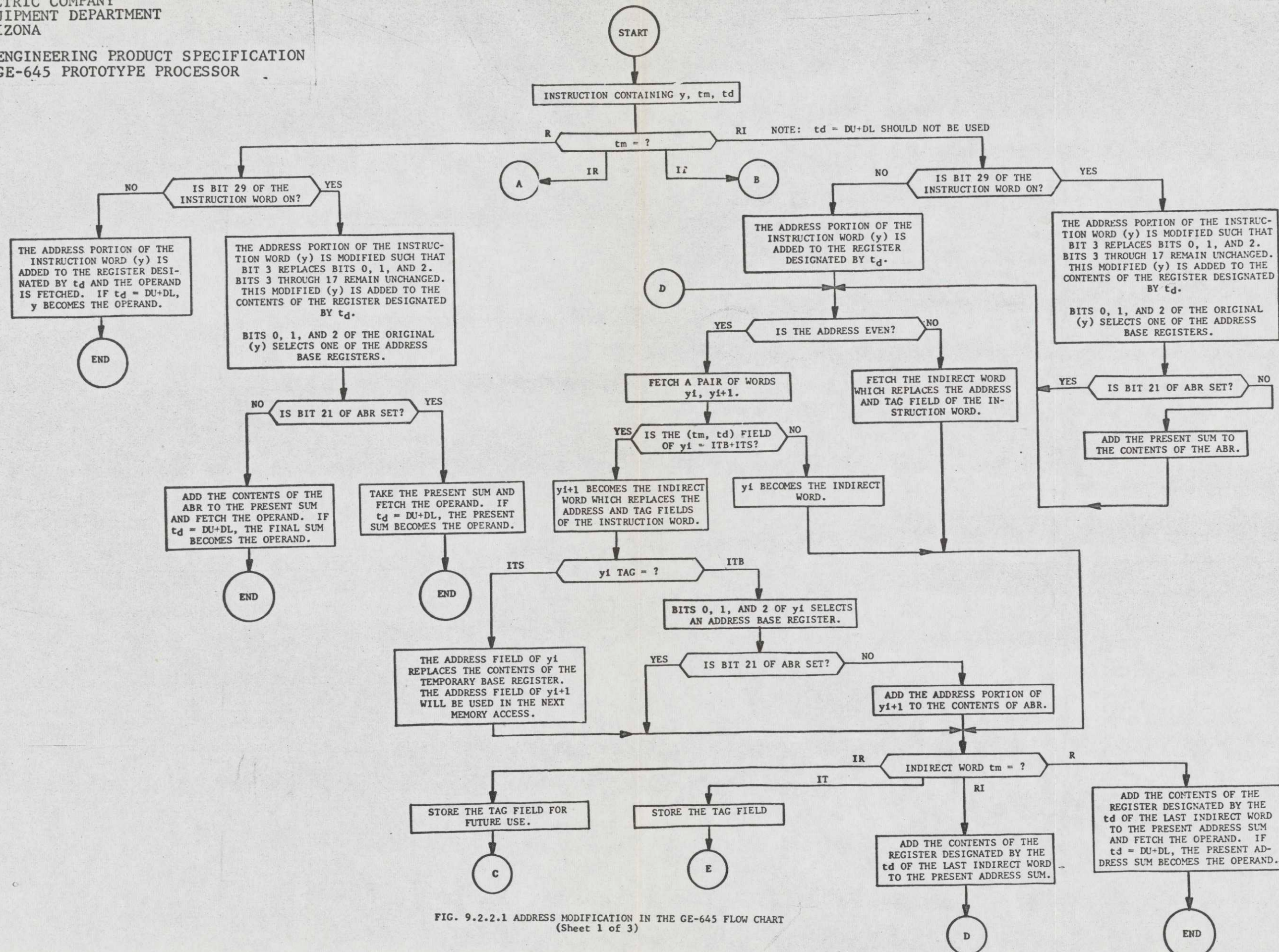


FIG. 9.2.2.1 ADDRESS MODIFICATION IN THE GE-645 FLOW CHART
(Sheet 1 of 3)

ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Spec. No. M50EB00107
 Cont. on Sh. 9-25 Sh. No. 9-24

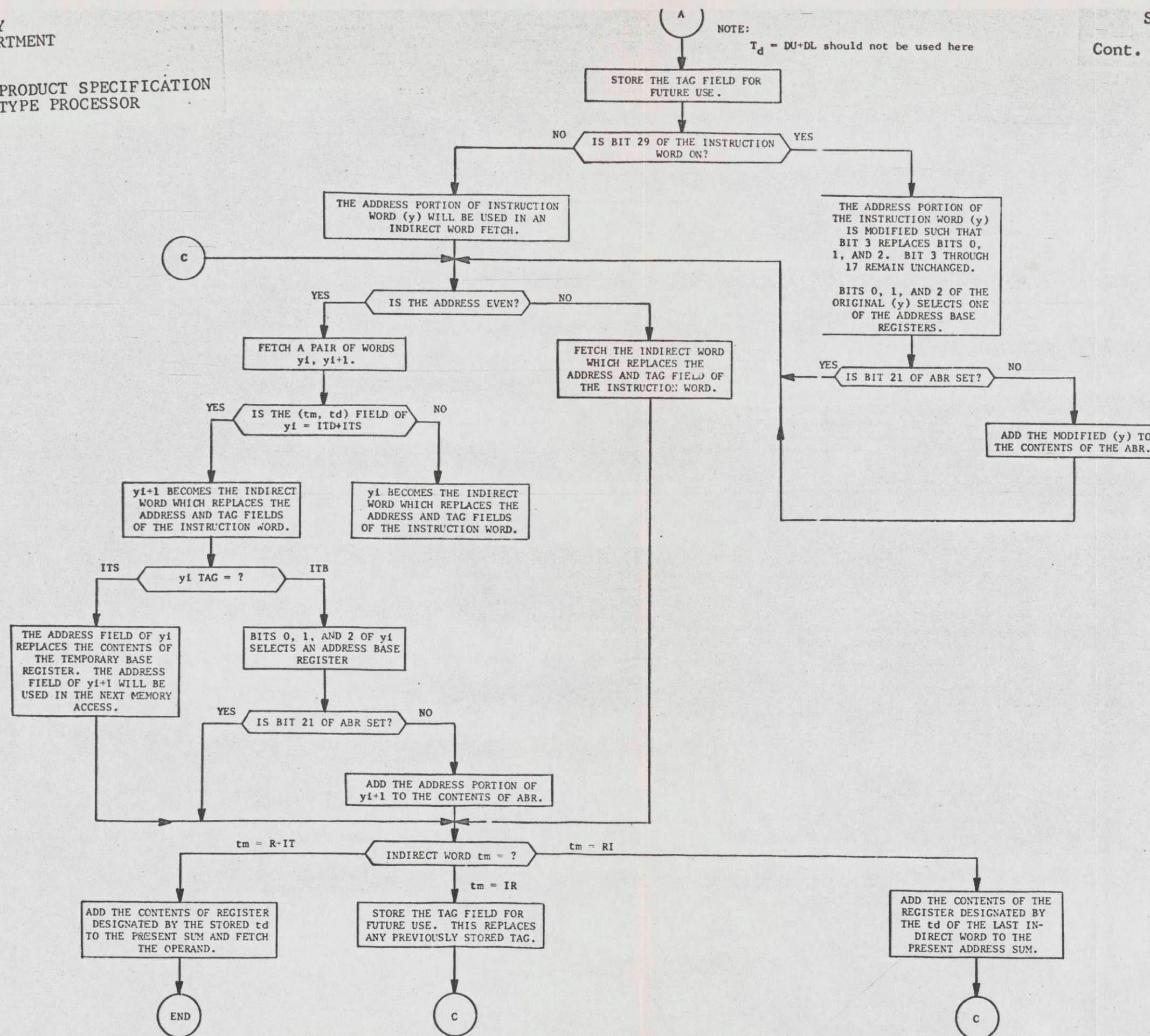


FIG. 9.2.2.1 ADDRESS MODIFICATION IN THE GE-645 FLOWCHART
 (Sheet 2 of 3)

ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

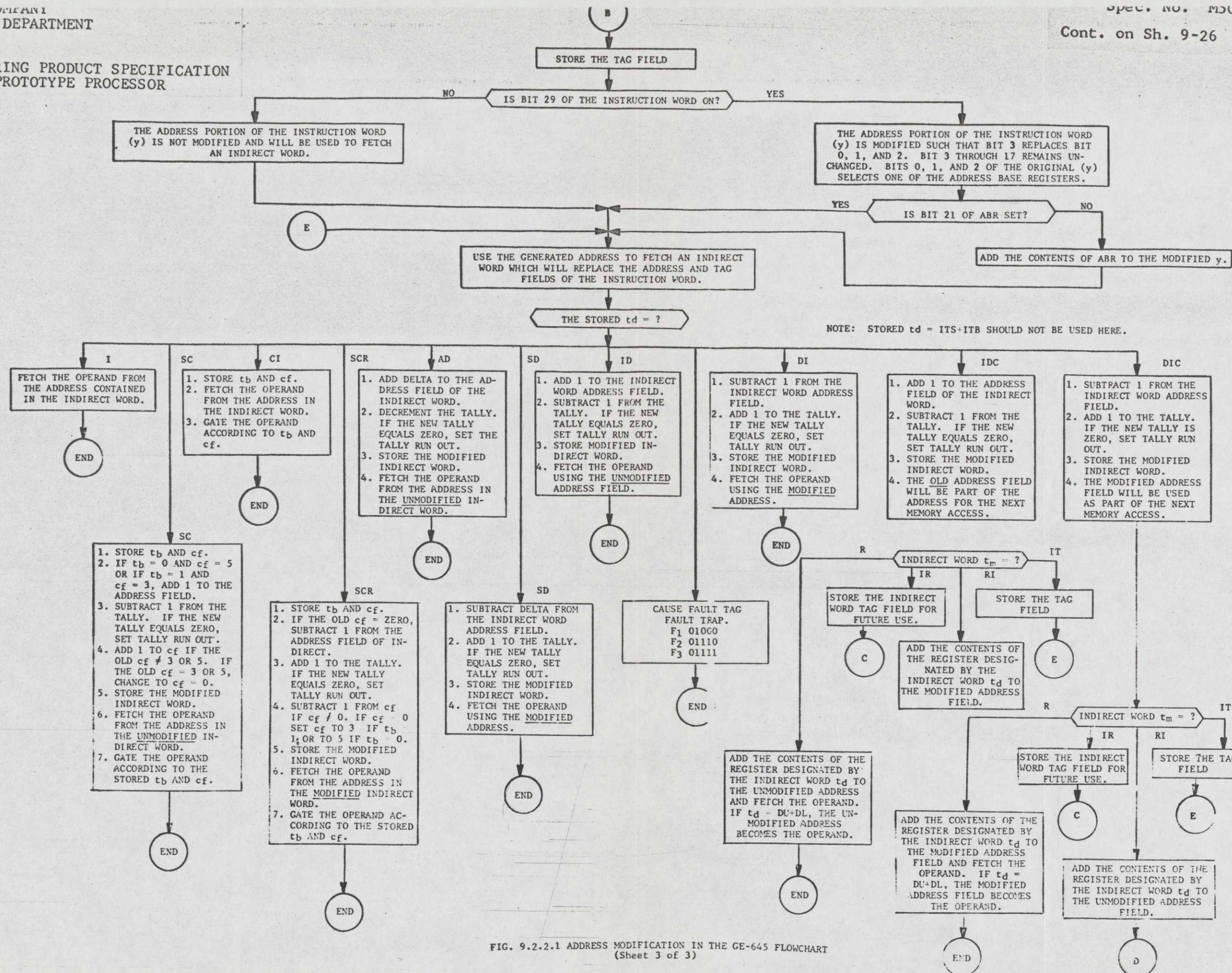


FIG. 9.2.2.1 ADDRESS MODIFICATION IN THE GE-645 FLOWCHART
(Sheet 3 of 3)

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-27 Sh. No. 9-26

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.2.1 - contd

If bit 29 of the instruction word is "1," and an internal base is designated by bits 0-2 of the instruction word, then the address field of the internal ABR is added to the address in the BS-adder during the PA prepare address cycle for an operand. Whenever an ABR is designated in an instruction word (bit 29 equals a "1"), bit 3 of the instruction word is extended to fill bits 0-2. This is done at the input to the YS-adder.

RI (Register then Indirect) Modification

For RI modification ($t_m = 01$), the register specified by t_d of the instruction word tag is used to modify the operand address in the same manner as previously discussed for the R modification. However, after adding the specified register and internal base register if specified, the effective address is then used to fetch an "indirect word" (a new word from memory that is the result of address modification). This "indirect word" replaces portions of the original instruction word in the Y- or C- register as follows:

- bits 0-17 replace the address
- bits 18-29 are ignored (op code of original remains)
- bits 30-35 replace the tag (t_m, t_d)

Any address modification called for by this indirect word is then executed. If an R modifier is called for in the indirect word, then the indirection terminates after the designated register is added. The effective address is then used to fetch the operand. Naturally, the appending of the various ABR's, the PBR etc. in the Interface Frame to form the memory address is performed as necessary for all memory accesses unless the Processor is in Absolute mode.

When any modifier is found in the t_m field of the new tag brought in by the indirect word, the indirection process continues as specified for an RI, IR or IT modification, until an R modifier is found which ends the chain. Also, whenever IR or RI modification is specified and the effective address in the BS-adder designates an even location, two indirect words are

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-28 Sh. No. 9-27

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.2.1 - contd

pulled in anticipation of an ITS or ITB modifier in the even indirect word. The first indirect word is strobed into the working register (Y or C) in the normal manner, and if it specifies ITS or ITB modification, then the odd indirect word of the pair gets strobed on top of the first (even) indirect word. If no ITS or ITB modification is detected, then strobing of the second (odd) indirect word is inhibited.

IR (Indirect then Register) Modification

When performing indirect then register modification ($t_m = 11$) the operand address, from the instruction word now present in the BS-adder, is used to fetch an indirect word. An internal base may be added to the instruction word address field prior to the first indirect word fetch if so specified by bits 0-2 of the instruction word address field. Any modification to be performed is as indicated by the t_m, t_d portion of the original word, which is stored in the CT-register just prior to the time that an indirect word is fetched from memory. When the indirect word is brought in from memory, it is strobed into the Y- or C-register depending on whether the even or odd instruction is being processed. If the t_m field of the indirect word has an R or IT modifier, then the t_d field of the original word that was stored in the CT-register is used to select the register, via the CT-switch and ZX decoder, which modifies the indirect word address. A second indirect word is then fetched from memory and strobed into the Y- or C-register. Thereafter, operation is as specified for RI modification. When an IR modifier is detected in the indirect word resulting from an IR modifier in the instruction word, then the new t_m, t_d field replaces the old t_m, t_d field in the CT-register. Like RI modification, if the indirect word is in an even location, an even/odd pair of words are pulled in anticipation of an ITS or ITB tag in the even word of the pair.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.9-29 Sh. No. 9-28

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.2.1 - contd

IT modification ($t_m = 10$) involves using the operand address in the instruction word to fetch an indirect then tally word (except for modifications F1, F2, F3), then operating on the location specified by the indirect word according to the operation code and tally designator (t_d) of the original word. For IT modification, any one of 13 variations specified by the t_d field are possible. The ITS and ITB modifications involve both the t_m, t_d field of indirect words pulled as a result of RI or IR modification. These can really be considered an Indirect Pair modification and do not fall in any one of the four defined types (R, RI, IR, IT) even though the t_m, t_d fields fall in the IT modification code range.

Indirect then tally words fall into four general categories depending on how the tag (t_m, t_d) of the instruction word, or indirect then tally word is interpreted:

- 1) I, DI, ID, F1, F2, F3 -- these tally designators are ignored in the indirect then tally word but are specified by the t_d field of the instruction word.
- 2) DIC, IDC -- these designators in the instruction word cause the t_m, t_d field of the indirect then tally word to be interpreted as a normal t_m, t_d and may designate R, RI, IR, or IT modification.
- 3) CI, SC, SCR -- these designators in the instruction word cause the t_m, t_d field of the indirect then tally word to be interpreted as a character size and character position for the operand specified by the address portion of the indirect then tally word.
- 4) AD, SD -- the tag field of the indirect then tally word is interpreted as a delta which is to be added or subtracted to the address of the operand.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.2.1 - contd

The tally portion of the indirect then tally word is contained and updated in the Interface Frame. The tag portion is ignored, is strobed into the CT-register, is sent to the Operations Unit and Interface Frame, or is added to the operand address in the YS-adder, dependent on the specific tally designator and the operations involved.

- 1) F1 (0000), F2 (0110), F3 (0111) -- detection of these designators in the instruction word causes an immediate fault sequence to be initiated in the Processor. This results in a "brute forced" XED instruction in the Y- and C-registers which generates a fault vector address for the specific fault tag; F1, F2 or F3. These fault tags all cause the Control Frame to respond in the same manner, the only difference being in the fault vector address associated with each tag.
- 2) I (1001) -- This designator results in the fetching of an indirect word using the address in the instruction word that is also present in the BS-adder. The resultant indirect-word address is strobed into the address portion of the Y- or C-register and the tag portion is ignored. Fetching of the operand is accomplished using the address portion of the indirect word now present in the BS-adder. (The YS- and BS-adders add whatever is presented to their inputs).
- 3) DI (1100) -- When a DI modifier is detected, the address in the BS-adder is used to fetch an indirect word which consists of an address (bits 0-17), a tally (bits 18-29), and a tag. The address portion is strobed into the Y- or C-register, depending on the location of the original instruction. The tally portion is strobed into the RS-adder in the Interface Frame, and the tag portion is ignored. The new operand address is decremented by "1" and the tally portion is incremented by "1." The resultant new address and tally are rewritten back into the original memory location of the indirect word, then the operand is fetched with the address

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-31 Sh. No. 9-30

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.2.1 - contd

obtained from the modified indirect word (original address minus "1") now present in the BS-adder. Decrementing of the operand address takes place in the YS-adder, and the decode of the DI modifier is taken from the CT-register outputs. The CT-register receives the instruction word tag just prior to the indirect cycle for the indirect then tally word. Every time that the indirect then tally location is accessed by the instruction word, the address of the indirect then tally word is decremented by "1" and the tally field is incremented by "1." When the tally reaches zero the Tally Run-out Indicator is turned on.

- 4) ID (1110) -- This modifier is essentially the inverse of the DI modifier. The operand address in the instruction word is used to fetch an indirect then tally word in the same manner as for DI modification. However, the address field is incremented by "1" and the tally field decremented by "1" before rewriting it in the memory location from which it was obtained. Then the operand is fetched using the original address of the indirect then tally word that is now present in the BS-adder from the Y- or C-register. Incrementing of the operand address contained in the indirect then tally word is done in the YS-adder. As soon as the modified address is rewritten back into memory the original address is restored. This is because "1" is removed from the YS-adder input and only the indirect then tally word address is still present. When the tally field reaches zero the Tally Runout Indicator is turned on.
- 5) DIC (1101) -- The DIC modifier is the same as the DI modifier with the following exception: the tag portion of the indirect then tally word brought into the Y-or C-register is treated as a normal tag, after the address and tally portions of the indirect word are updated and rewritten into the memory location from which it was obtained. The new tag is strobed into the CT-register and may specify R, RI, IR, or IT modification (R must = N); in which case modification is performed as specified.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.2.1 - contd

If no further indirect word was specified by the tag, then the operand is fetched using the address or the modified indirect word (original address minus "1").

- 6) IDC (1111) -- This modifier is the same as the ID modifier with the following exception: the tag portion of the indirect then tally word brought into the Y- or C-register is treated as a normal tag after the address and tally portions of the indirect word are updated, and rewritten into the memory location from which it was obtained. The new tag is strobed into the CT-register and may specify R, RI, IR or IT modification (R must = N); in which case the modification is performed as specified. If no further indirect word was specified by the new tag, then the operand is fetched using the address of the original indirect word still located in the Y- or C- register, and now present in the BS-adder. When the tally portion of the indirect word reaches zero, then the Tally Runout Indicator is turned on.
- 7) ITS (100011) and ITB (100001) -- These modifiers are different than the normal IT modification since they are only recognized as a result of RI or IR address modification specified by the tag field of an instruction or indirect word that designates an even address. With this type of address modification, two words are pulled from memory, in a double-precision read-restore operation. The first word is unconditionally strobed into the Y- or C-register. Then the tag portion is decoded from the ZI_{12-17} lines for a possible ITS or ITB tag. If these tags are detected, the Control Frame stops any further address preparation until the second word of the pair is received from the memory. The second indirect word is a normal indirect word and is strobed on top of the first word that contained the ITS or ITB tag. Operand address preparation is now resumed in the normal manner, but with the new indirect word that is relative to a new address base. For ITS modification, the new base is strobed

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.2.1 - contd

into the TBR in the Base Frame; for ITB modification the new base is referenced from the segment tag registers in the Base Frame which now contain a new segment tag brought in by the ITB modification. The new base specified by the segment tag register in the Base Frame is then added in the BS-adder in the Control Frame if the ITB tag specified an internal base.

In summary: ITS and ITB modification is a method of changing the address base or "pointer" to a different address base; whether it be to a new segment or a different base within a segment. The Control Frame receives the first indirect word in the conventional manner, decodes the tag from the Y- or C-register, and if ITS or ITB modification, holds up operand address preparation until the second indirect word is brought in on top of the first. When no ITS or ITB tag is detected the second indirect word is ignored.

- 8) CI (1000) -- With this modifier, an indirect then tally word is obtained from the address contained in the instruction word. The indirect word address field replaces the operand address of the instruction word in the Y- or C-register, and the tag portion goes to the Operations Unit or the Interface Frame, depending on whether the operation to be performed is a Load or Store operation. The t_m field of the tag of the indirect then tally word defines a 6-bit or 9-bit character to be operated upon, and the t_d field defines the particular character involved. Fetching of the operand character is accomplished by using the operand address now present in the BS-adder from the Y- or C-register.
- 9) SC (1010) -- This modifier deals with 6-bit and 9-bit operand character sequencing. The instruction word address is used to fetch an indirect then tally word consisting of an operand address, tally, and tag field respectively. Only the operand address is strobed into the Y- or C-register. For

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-34 Sh. No. 9-33

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.2.1 - contd

SC modification, the tag field of the indirect then tally word denotes the particular character or byte to be operated upon. Whenever this indirect then tally word is referenced, the byte position is increased by one, the tally is decreased by one, and it is rewritten back into the memory location from which it was obtained. When the tally field reaches zero, the Tally Runout Indicator is turned on. The byte position will progress from zero, to three or five and then start over from zero.

When the byte position goes from five to zero (6-bit bytes) or three to zero (9-bit bytes) the address of the operand is increased by one to obtain the memory location of the next operand. This is accomplished by decoding the byte position from bits 33-35 on the ZDI lines as the indirect then tally words are brought in from memory, and adding +1 to the address in the YS-adder when the byte count reaches maximum (5 or 3 indicating 6 or 4 bytes). Operation on the byte is done using the original byte specified by the first indirect word.

- 10) SCR (0101) -- SCR modification is the inverse of SC modification. The indirect then tally word is brought into the Y- or C-register in the same manner. But for SCR modification, whenever the indirect word is referenced, the byte position is decreased by one, the tally field is increased by one, and the new information is written back into the location from which it was obtained. Whenever the tally field reaches zero, the Tally Runout Indicator is turned on. Operation on the byte position is done using the new character position and new address. As before, the tag of the indirect then tally word is decoded from the ZDI lines as the words are brought from memory. Whenever zero is detected, -1 is added to the address in the YS-adder, and the tag field indicating the byte position is set to maximum (5 or 3 for 6 or 4 bytes).

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.2.1 - contd

- 11) AD (1011) -- With this type of address modification the instruction address is used to fetch an indirect then tally word containing an operand address, tally, and delta field; delta occupying bits 30-35 of the word. The operand address is strobed into the Y- or C-register, and the delta field is routed through the V portion of the ZX switch to be added to the operand address. The tally is decreased by "1." When the tally field reaches zero, the Tally Runout Indicator is turned on. The operand is then fetched using the original address contained in the indirect then tally word that is still present in the Y- or C-register.
- 12) SD (0100) -- This modification is the inverse of AD. Each time the indirect location is accessed, the operand address is decreased by delta, the tally is incremented by one, and they are rewritten back into the location from where they were obtained. When the tally reaches zero the Tally Runout Indicator is turned on. The operand is now fetched using the modified address still present in the YS-adder corresponding to the updated indirect then tally word. Subtracting delta is done through the $\bar{V}$ and -I portion of the ZX switch which have as their inputs the delta portion of the indirect word from the DV 00/35 OB (ZDI) data input lines and logic 1's. To subtract, the 2's complement of delta must be added in the YS-adder.

9.2.3 INSTRUCTION EXECUTION MODES

The modes of execution for the Processor which were described in paragraph 2.3.3, are defined by two flip-flops in the Control Frame designated MSY and MSI. These flip-flops indicate that the instructions fetched from memory, and now occupying the Y-, C-, and I-registers, were fetched from a Procedure-Master segment; or that the Processor is in the Temporary Absolute or Absolute mode of address. Information concerning segment types is sent from the Interface Frame and is defined by the descriptor field of a Segment Descriptor Word or Page Table Word in the descriptor register.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.9-36 Sh. No.9-35

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.3.1 MSI (Master in I-Register)

In the Append mode the MSI flip-flop being set indicates that the instructions contained in the I-register were fetched from a Procedure-Master segment. This flip-flop is normally reset since the majority of segments available to a "user" are not Procedure-Master. However, whenever instructions are being fetched to fill the I-register, the strobe that strobes the even word of the pair into the I-register, bits 0-35, also strobes the MSI flip-flop. If the descriptor field of the SDW or PTW contained in the descriptor register in the Interface Frame indicates Procedure-Master, MSI is set; otherwise it is reset. Whenever an RCU instruction is being executed, MSI may be changed to reflect the stored RCU data.

MSY (Master in Y- and C-Register)

In the Append mode this flip-flop indicates that the instructions now in the Y- and C-registers that were in the I-register or were brought in from the ZDI lines, were fetched from a Procedure-Master segment. Whenever the Processor is in the Temporary Absolute or Absolute mode of address, the Execution mode is forced to master. If the instruction fetch to fill the Y- and C-registers is the result of an XED instruction (which is not the result of a fault or an external interrupt) then the MSY flip-flop may not change until the XEDed instructions are executed.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.9-37 Sh. No.9-36

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.4 INSTRUCTION FETCHES

The fetching of instructions for the GE-645 Prototype Processor is initiated and controlled by the Control Frame. Since the normal condition of the Control Frame is to keep four instructions in the instruction registers at all times, the sequences become very involved in the cases of instructions causing a transfer of control (faults all transfers, plus the RET, RTD, RCU, XEC and XED instructions). In addition, to pick up additional speed in cases where there is a load-store instruction combination in the I-register, the instruction fetch for reloading the I-register is postponed until after the operand address preparation cycle of the "load" instruction. There are many other peculiarities which can cause the instruction fetch sequence to be altered slightly. These sequences will be covered in detail in paragraph 9.4. A flow chart of the "normal" instruction fetch sequence is shown in Fig. 9.2.4. This flow chart shows a normal two-instruction, or four-instruction fetch with the possibility of a load-store instruction combination, or transfer instruction in the I-register, and the possibility of an XED instruction in the Y- or C-registers.

Referencing both Fig. 9.2.4 and 43D160212 sheet 5, assume that the Processor has been initialized in some manner (discussed in the section on fault logic) and starts to fetch instructions. Normally starting out will require a four-instruction fetch (two at a time). The Control Frame enters a PI cycle for the instructions, and the contents of the ICTB-register are switched to the YS-adder input. The resultant address to fetch the instruction pair is the address from the BS-adder which is sent to the Interface Frame to fetch the instruction pair. Address appending may or may not take place in the Interface Frame, depending on the state of the Control Frame's absolute flip-flop. When the instruction address is sent to the Interface Frame, the Control Frame enters into a WI₂ cycle to wait for the instruction, ICTB is moved into ICTC, and +2 is added to ICTB (+1 added in both the YS- and BS-adders). Instructions are normally fetched in pairs and when the instructions come from memory, they are loaded into the I-register.

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

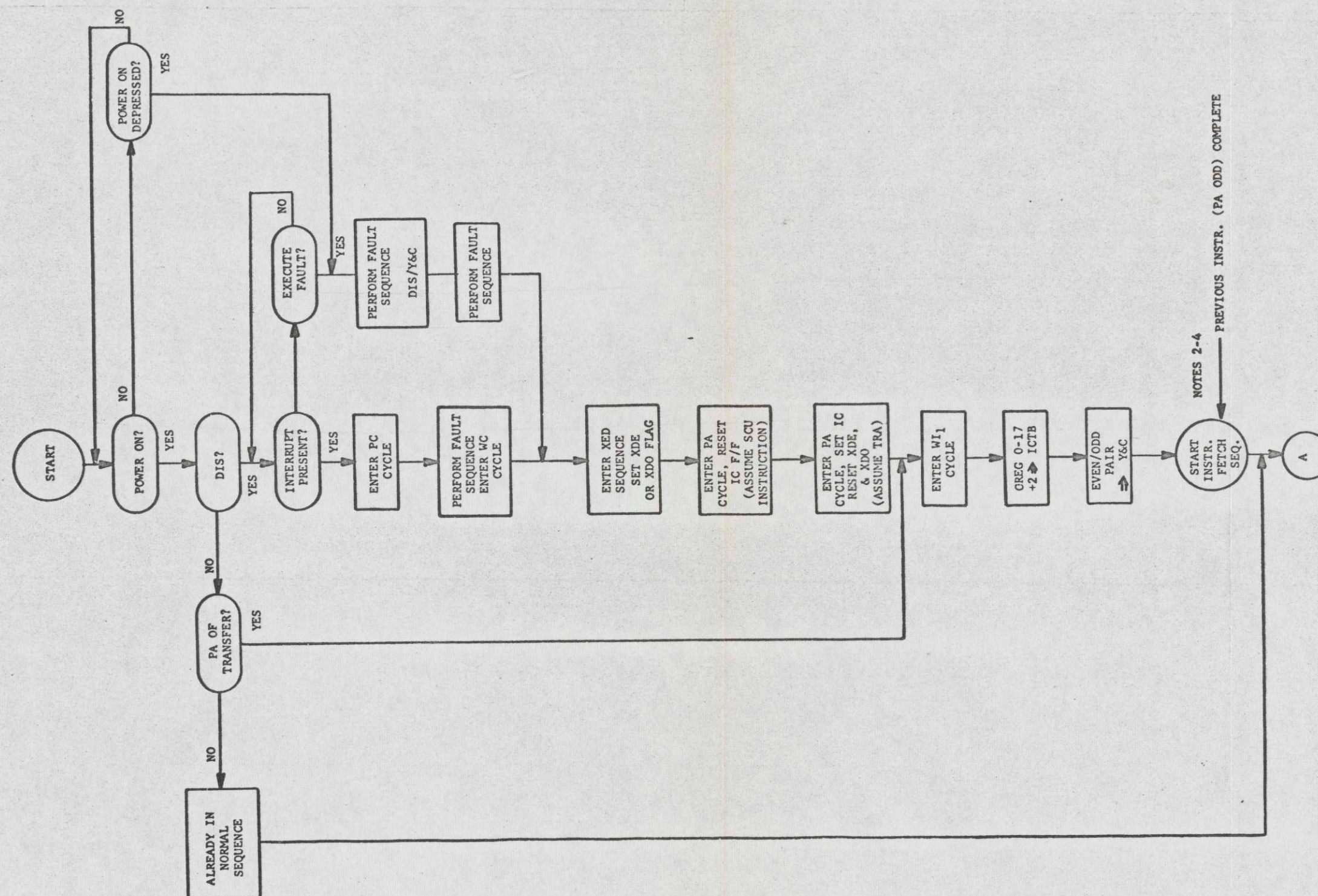


FIG. 9.2.4 GENERAL INSTRUCTION FETCH SEQUENCE,
 FLOWCHART (sheet 1 of 2)

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

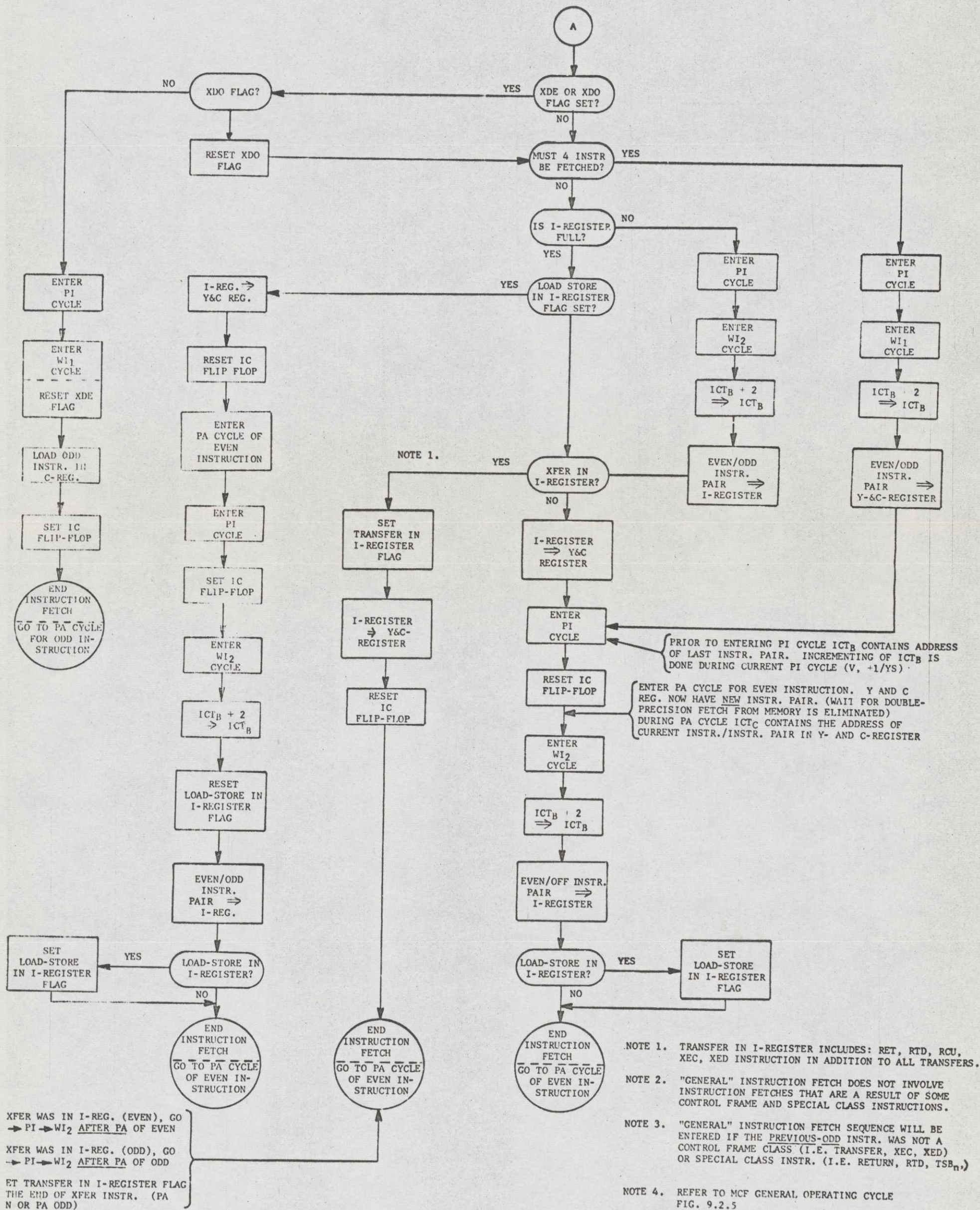


FIG. 9.2.4 GENERAL INSTRUCTION FETCH SEQUENCE, FLOW CHART (sheet 2 of 2)

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.9-40 Sh. No. 9-39

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.4 - contd

If the Y-, C- and I-registers are full, and there is a load-store instruction combination in the I-register, the fetching of a pair of instructions to fill the I-register after the I-register contents are moved into the working registers, is postponed until the time between the PA cycle for the load type instruction and the PA cycle for the store type instruction. This allows the Control Frame to take advantage of the relatively long time between the load- and store-instruction execution. When an XDE or XDO flag is set, indicating an execute double instruction is in the even or odd instruction register, the instruction fetch sequence is a little different. For an XED instruction in the even instruction location, two words are pulled from the address specified by the XED instruction during the PA cycle of the XED instruction, executed, then the instruction in the C-register that was destroyed by bringing in the second XEDed instruction is refetched. When an execute double instruction is in the odd instruction location, the XEDed instructions are fetched during the PA cycle of the XED instruction, executed, then four instructions must be pulled in the normal manner for a four-instruction fetch.

9.2.5 OPERAND FETCHES

As mentioned previously, operand fetches within the Control Frame fall into five general classes: Normal OU; Direct OU; Control Frame; Base Frame; and Specials. Instruction in each class all, except the last class Specials, cause the Control Frame to respond in essentially the same manner. Each of the instructions in the "Specials" class cause the Control Frame to react differently, depending on the instruction involved. Figure 9.2.5 is a very generalized flow chart of the major sequences involved for each of the five classes. Included in the table on Fig. 9.2.5 are the different instructions in each class. Generally speaking, each class involves going through the same sequences for each of the instructions of that class. The sequences can become quite involved and overlapped, since instruction and operand address preparation, in addition to operand

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-41 Sh. No. 9-40

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.2.5 - contd

execution, can go on at the same time for a maximum of three instructions before the Operations Unit completes the first instruction. In addition, the possibility of faults occurring in various phases of the sequence have been left out. All the detailed sequences will be covered beginning in paragraph 9.4, in addition to how each "piece" of the sequence involves the hardware elements explained in paragraph 9.3.

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

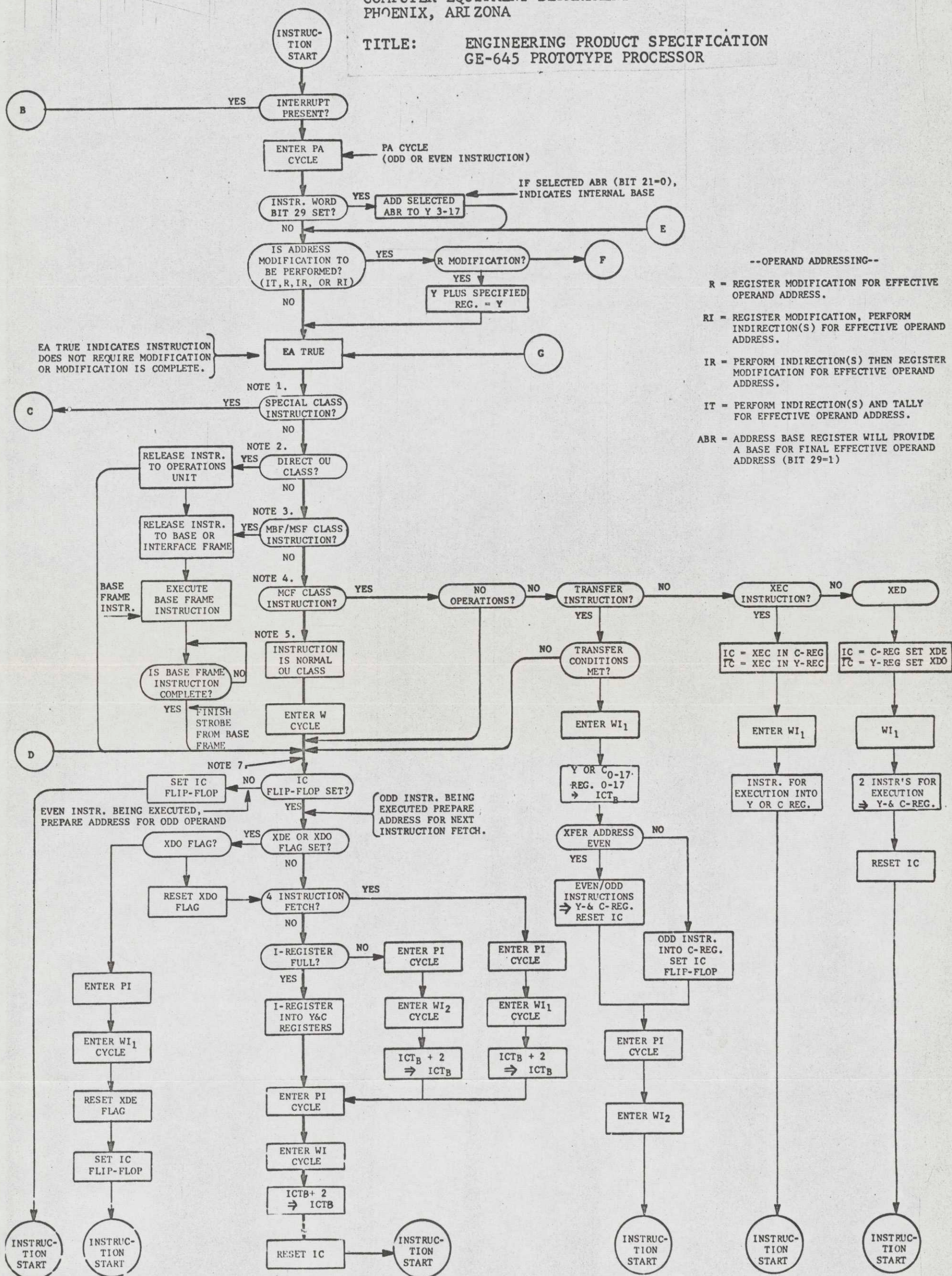
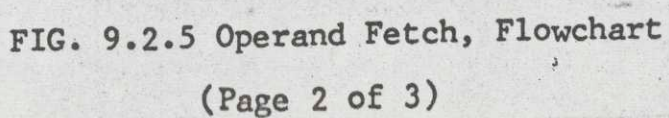


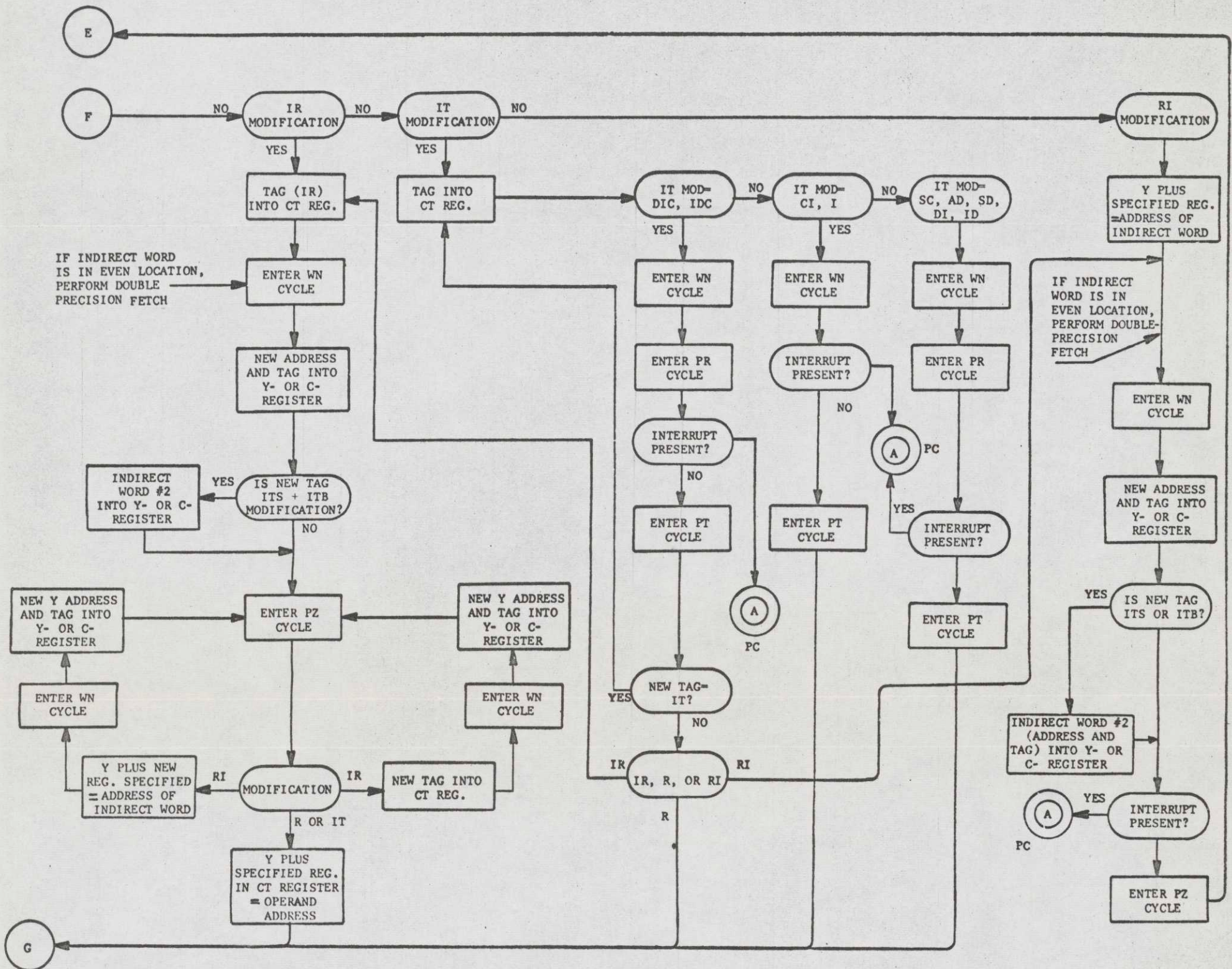
FIG. 9.2.5 Operand Fetch, Flowchart
(Page 1 of 3)

Spec. No. M50EB00107
Cont. on Sh. 9-41.1 Sh. No. 9-41

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR



TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR



--NOTES--

- 1. SPECIAL CLASS INSTRUCTIONS ARE THOSE WHICH INVOLVE MULTIPLE FRAMES AND INDIVIDUALLY DETERMINE THE MCF SEQUENCE MODE.
- 2. DIRECT OU CLASS INSTRUCTIONS ARE THE OU INSTRUCTIONS THAT DO NOT REQUIRE MEMORY ACCESS FOR OPERAND.
- 3. MBF/MSF CLASS INSTRUCTIONS ARE THOSE WHICH INVOLVE THE BASE AND/OR ASSOC. MEMORY FRAMES, AND FOR THE MOST PART ARE EXECUTED OUTSIDE THE CONTROL FRAME.
- 4. MCF CLASS INSTRUCTIONS ARE THOSE WHICH ARE EXECUTED PRIMARILY WITHIN THE CONTROL FRAME.
- 5. NORMAL OU CLASS ARE THOSE OU INSTRUCTIONS WHICH REQUIRE AN OPERAND TO BE FETCHED FROM OR SENT TO MEMORY.

SPECIAL	DIRECT OU	MBF/MSF	MCF	NORMAL OU
SCU *	SHIFTS	ADB _n	TRANSFERS	ARITHMETIC
STCD *	GTB	EAB _n	NOP	OU LOAD'S
RCU *	NEG	EAP _n	XEC	OU STORE'S
RET	NEGL	LBR _n	XED	LOGICAL
RTD *	FNO	LDB	TSB _n *	BCD
	FNEG	LDBR		
CIOC	EAA	LDCF		RMCM
MME 1-4	EAQ	SBR _n		SMCM
DRL	EAX _n	SDBR		SZN
RPT		STB		LXL _n
RPD		STP _n		SXL _n
DIS		CAM		
		SAZ		
		SAM		

* INVOLVE BASE FRAME

- 6. HEAVY LINE INDICATES "NORMAL" PATH OF CONTROL FRAME OPERATION, FROM INSTRUCTION INITIATION TO SUBSEQUENT INSTRUCTION FETCH. "NORMAL" OPERATING CYCLE IS ASSUMING A NORMAL OU INSTR. WITH NO ADDRESS MODIFICATION.
- 7. OPERAND IS FETCHED OR STORED FOR OU DURING W CYCLE. CONTROL FRAME IS AVAILABLE FOR NEXT INSTRUCTION/OPERAND FETCH AT END OF W CYCLE.

FIG. 9.2.5 Operand Fetch, Flowchart
(Page 3 of 3)

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.9-44 Sh. No. 9-43

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3 PRINCIPLE HARDWARE ELEMENTS AND FUNCTIONS

The following paragraphs explain the operation of the principle hardware elements and functions in the Control Frame that can be defined by a definite hardware physical relationship (for example, a register, counter, etc.) or a functional grouping of circuits (for example, strobe generation circuits and interface term logic, Z-function, etc.). The sequence of operation and relationship between all elements and functions is covered in detail in paragraph 9.4.

9.3.1 STROBE \$R, \$C, \$ΔAM1, \$ΔAM2, \$IF, AND INTERFACE TERM
(See 43D163387, sheets 2,3,4)

Strobes \$C and \$R are the two most widely used strobes in the Control Frame. Strobe \$C is utilized more extensively than any other strobe and is generally concerned with the setting and resetting of the sequence flags (PA, PZ, PN, PT, IC etc.); while strobe \$R occurs only if an interrupt is sent to the Memory Controller. Strobe \$R is used to set and reset the flags concerned with the interrupt process. Strobes \$ΔAM1, \$ΔAM2, and \$IF are used to provide time delays to: enable instruction decodes and the Z (Store-Compare) function to stabilize; allow the BS-adder to stabilize; start the Interface Frame; and generally hold up the development of further strobes until certain functions in other frames have had a chance to be performed and become stabilized. The functions of strobes \$ΔAM1, \$ΔAM2, and \$IF will become clearer during the discussion of the interface term (a composite equation), which is developed from a number of conditions indicating whether all of the affected areas within the Processor are ready to proceed with certain sequences. Since the timing in many areas of the Processor is asynchronous, the interface equation is quite large. For this reason the interface equation is explained in detail in paragraph 9.3.1.2.

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.1.1 Strobe \$C and \$R Generation (See 43D163387, sheet 2)

An examination of the two pulse drivers that generate \$C and \$R show that they have three common signal inputs, \$ABT, \$PRI, and \$PRII. In addition, \$C may be generated by \$CDA or \$DS-PR). Thus it should be clear that \$C may occur alone, but \$R may never occur without \$C also being generated.

Strobe C - Strobe \$C may be generated under any one of the five following conditions:

- 1) Receipt of \$CDA, which is a pulse derived from the data-in control logic used to load the Y- and C-registers (see 43D163387 sheet 24). For a normal instruction fetch, when the Y-register is loaded with the even instruction of a pair:

$$\$CDA = \$DA_1 \cdot DYCA \cdot (PR \text{ or no } P \text{ cycle})$$

Level DYCA is from a flip-flop which sets whenever an instruction word is to be brought into the Y- or C-registers. Strobe \$DA₁ is generated in the Control Frame after its reception from the Interface Frame, and indicates that data is on the ZDI lines from memory.

- 2) Strobe \$DS and PR are present. These terms will be true whenever the Control Frame is in the PR cycle for some IT address modification. Level PR is the prepare rewrite flag, and \$DS is from the Interface Frame indicating that data has been loaded into the Data-Out Register in the Interface Frame, to be later stored in memory.
- 3) Strobe \$ABT is received from the base frame fault logic as a result of the WF (Wait for Fault) flip-flop in the Base Frame being set. The WF level indicates that either an external interrupt has occurred and will be recognized, or a fault has occurred. If WF is set, the Control Frame will have already performed a "snapshot" routine to safe-store the current status of the Control Unit. The "snapshot" sequence is explained in detail in later paragraphs. With the receipt of \$ABT, \$C and \$R are generated to allow an interrupt to be set to the Memory Controller via the Interface Frame to complete the interrupt routine.

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GENERAL ELECTRIC COMPANY
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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-46 Sh. No. 9-45

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.1.1 - contd

- 4&5) Strobes \$PRI or \$PRII are received. These strobes are nearly identical in their source. However, \$PRI is inhibited if the Interface Frame has detected a fault; whereas \$PRII is generated only if a fault occurs.

$$\begin{aligned} \$PRI \text{ (See 43D163380 sheet 6)} &= \$PRC \cdot \overline{APE} \cdot \overline{ISR} \cdot \overline{SPF} \\ &+ \$TEST \cdot RST \end{aligned}$$

where:

$$\$PRC = IFR \cdot SPR \cdot BFR \cdot \overline{RR} \cdot CFR$$

and

(See 43D163387 sheet 2)

$$\$PRII = IFR \cdot SPR \cdot BFR \cdot RR \cdot CFR$$

The similarity at the origination of \$PRC and \$PRII is readily apparent since $\overline{RR}$ and RR are the only differences. The term RR will be true for certain faults detected by the base frame fault logic and will inhibit \$PRC, but will allow \$PRII. This is to allow the Control Unit to complete certain procedures even though the rest of the machine will be halted. Strobe \$PRII will generate a \$R to enable the Operations Unit to complete its operations, but \$INT to the Memory is inhibited. If \$PRC is allowed to go to the Interface Frame ($\overline{RR}$ present), then the Interface Frame can still inhibit \$R and also \$INT for a fault. The terms that must be present to generate \$PRI from \$PRC in the Interface Frame include $\overline{APE}$ (not appending parity error), $\overline{ISR}$ (not inhibit \$R), and $\overline{SPF}$ (part of the manual program step circuits for test purposes). The terms for \$TEST and RST enable the generation of \$PRI in the test mode of operation where the Processor is being manually stopped. When \$PRC is not inhibited in the Interface Frame, it emerges a \$PRI, which subsequently generates \$C and \$R resulting in an interrupt to continue the normal sequence.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-47 Sh. No. 9-46

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.1.1 - contd

Re-examining the gated pulse amplifiers which generate $\$PRC$ and $\$PRII$, one finds that they are identical except for RR and RR , which has been explained. The other terms concerned are:

IFR -- interface frame ready, which is set by $\$IFF$ from the Interface Frame and generally is the last condition to be brought up. Strobe $\$IFF$ specifies that the Interface Frame has a final address and is ready to send a $\$INT$ to memory.

SPR -- this level is a flip-flop used only for test and step purposes and will normally be set.

BFR -- base frame ready flip-flop, which is set by $\$BC + \$PRR (PN + BFI) + (EA \cdot BFI \cdot \$PRR)$. Strobe $\$BC$ comes from the Base Frame and signals the completion of a base frame instruction. Strobe $\$PRR$ is generated by the interface term coming true. If there is not a base frame instruction, the BFR is set almost as soon as the Control Frame starts a preparation cycle. Finally, if there is a base frame instruction but the effective address has not yet been prepared, $\$PRR$ will set BFR. The BFR flip-flop may not be set by $\$BC$ if any indirections or appending is required, since the Base Frame is not started by the Interface Frame until an $EA \cdot FA$ are present and hence no $\$BC$ to set BFR is generated.

CFR -- control frame ready is the last term necessary and is a direct result of the interface term ($INTR$) coming true. CFR is almost always the first flip-flop set, except if BFI is present. Strobe $\$PR$ unconditionally sets CFR.

$$\$PR = \$PCFF (54 \text{ or } 126 \text{ nanoseconds after } \$PCFF) \cdot \overline{CSR}$$

where:

$$\$PCFF = \$PRR (36 \text{ or } 18 \text{ nanoseconds after } \$PRR) \cdot \overline{ONC}$$

and

$$\$PRR = INTR \text{ (Interface term via a 301 pulse amplifier)}$$

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-48 Sh. No. 9-47

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.1.1 - contd

The times in the parentheses for \$PR are the differences between the time that a \$LAST from the Operations Unit is being processed by the Control Unit, and no \$LAST is received; the longer time being for \$LAST. Strobe \$LAST is used to generate a strobe to count the TMCH counter down. The TMCH counter is used to keep track of the number of operation codes sent to the Operations Unit for execution. The possibility exists that the TMCH counter can be counted up and down at the same time. Hence, the longer delay for \$PR, when SLO/FST is set, to provide time for possible counting of TMCH down before being counted up. The conditions involved are covered in more detail in the TMCH counter discussion paragraph 9.3.9. The term CSR is normally true unless a fault is detected or a fault operation code is detected after the interface equation has been satisfied.

The times shown in parenthesis for \$PCFF are the difference between the Control Unit in fast clock (determined by Maintenance Panel switch settings) and normal clock operation. The shorter time is used only for marginal timing tests of the Control Unit. If an Operation Not Complete fault is detected ONC is false and \$PCFF is inhibited.

Strobe \$R -- As mentioned previously, \$R is generated from \$ABT, \$PRI or \$PRII. These three conditions are the only ones that will generate \$R, and their meanings have already been explained under \$C generation.

9.3.1.2 Interface Term (INTR) (See 4.3.1.3.1, and 4.3.1.3.2)

The interface term combined equation (INTR) will become true if the required portions of the Processor are ready to proceed. This term may be brought up by any one of nine different enable conditions. The composite equation will be separated here for clarity, and the nine possible enable conditions will be examined first in the manner in which they produce INTR true (INTRB ANDOR) (provided INTR is not inhibited, see 4.3.1.3.2).

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-49 Sh. No. 9-48

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.1.2 Interface Term (INTR) (See 43D163387, sheet 4)

The interface term combined equation (INTR) will become true if the required portions of the Processor are ready to proceed. This term may be brought up by any one of nine different enable conditions. The composite equation will be separated here for clarity, and the nine possible enable conditions will be examined first in the manner in which they produce INTR true (BINTIB RNSO) (provided INTR is not inhibited, see 9.3.1.3):

1) $(TMCH = 0) \cdot (\overline{EA}) \cdot (\overline{STORES + RAR})$

If the TMCH counter equals zero the Operations Unit has completed its last instruction and the current instruction is not an Operations Unit store or read-alter-rewrite. (In other words, any instruction except stores or read-alter-rewrites.)

2) $EA \cdot (STORES + RAR) \cdot SDY$

An effective address is present for a store or read-alter-rewrite operation. The SDY term indicates that the Operations Unit has the data for the store operation, and the Control Frame may now begin to prepare for having the Interface Frame issue an eventual \$INT to Memory.

3) $(\overline{XDE + XDO}) \cdot PI$

The Control Frame is in a normal PI cycle, and the execute double even, and execute double odd flip-flops are reset indicating that the PI cycle is not the result of an XED instruction.

4) $TERM \cdot \overline{CSR}$

TERM is a level brought high when the Operations Unit terminates a "repeat" instruction. It may also be true if a fault condition occurs and the Processor does not request a memory cycle. The term CSR is normally not present unless a faulty operation code or a fault is detected and the processor fault logic has not had a chance to initiate a fault sequence. When CSR sets, \$PR is stopped and the

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.1.2 - contd

interface term is held off. For "repeat" instructions, when TERM is brought up during a fault initiated by SFF, SFF is forced off by TERM as long as the fault is not an Operations Unit fault. In other words, unless the fault is an Operations Unit fault and would effect the execution of the "repeated" instruction(s) it is ignored. As soon as CSR is set and pulls down SFF in conjunction with a TERM condition, CSR is forced reset allowing the Interface Term and \$PR (other conditions being equal).

- 5) $(EA) \cdot (Y+RSW) \cdot \overline{TAS} \cdot \overline{RPT'S} \cdot \overline{MFREEI} \cdot DBF \cdot (TMCH=1) \cdot \overline{BFI}$ EA.
(Y+RSW) -- indicates that an effective address for a direct operand is present; Y signifies the direct operand and, RSW is the read switches instruction which is also a direct operation.

$\overline{TAS}$ - indicates a "not test and step" condition.

$\overline{RPT'S}$ - means that the Control Frame cannot be doing any of the "repeat" instructions.

$\overline{MFREEI}$ - will be reset if the Operations Unit is ready to accept an operand.

$\overline{DBF}$ - indicates that a direct operand has not been loaded into the Direct Buffer in the Base Frame. The Direct Buffer holds the direct operand.

(TMCH = 1) - Indicates that the Operations Unit is still operating on the previous instruction but allows a direct operand to be loaded in the Direct Buffer even though the Operations Unit may be busy. If the Direct Buffer had been full DBF would be true and stop further action until the Operations Unit takes the operand.

$\overline{BFI}$ - This term is to prevent any overlap of Operations Unit and base frame instructions. If the Operations Unit is busy, the interface term is held off until TMCH = 0; then released (equation 1) to allow the base frame instruction to be completed.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-51 Sh. No. 9-50

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.1.2 - contd

$$6) (PA+PZ) \cdot (\overline{ZI=IT}) \cdot (\overline{FT+FD}) \cdot (\overline{EA}) \cdot (\overline{CT+DIS})$$

The Processor is preparing an indirect address (PA) or (PZ) of the IR or RI type. Terms $\overline{FT+FD}$ indicate not a repeat or repeat double instruction; EA has not been generated and there is not a conditional transfer or delay until interrupt instruction on the operation decode bus ($\overline{CT+DIS}$).

$$7) (SFF) \cdot (LPC) \cdot (DVK+FLF+SEP+BTPFOB)$$

This group of terms is for conditions where the Control Unit is waiting to service an Operations Unit or Control Unit fault. The terms DVK, FLF and SEP, are for Divide Check, Overflow and Parity, Operations Unit faults. Control unit instructions that cause faults are handled by BTPFOB which contains $TMCH = 0$. The idea behind equation 7, is that for Operations Unit and Control Unit faults, the Control Unit is allowed to continue and service the fault.

$$8) (TMCH = 1) \cdot (EA \cdot NOP \cdot \overline{ONR}) \cdot (ZI = \overline{IT})$$

These terms are to allow the Control Unit to do a "no operation" (NOP) instruction, $ZI = \overline{IT}$ is to inhibit the interface term for IT modifier and ONR inhibits the interface term until the 0-register in the Operations Unit is free.

$$\begin{aligned} 9) & [(TMCH = 1) \cdot (\overline{FT \cdot RF + FL}) & (9a) \\ & + (\overline{LREG} \cdot (\overline{FT+FD+FL}) \cdot TMCH = 2 \cdot (\overline{XDE+XDO}) \cdot Z2_4 = \text{SHORT}] & (9b) \\ & \cdot [(\overline{TAS} \cdot T \cdot \overline{STORE+RAR} \cdot \overline{RET} \cdot EA \cdot Y+RSW) & (9c) \\ & \cdot (\overline{BFI}) & (9d) \\ & \cdot (\overline{MDV} \cdot (ZI = \overline{IT}) \cdot EA & (9e) \\ & \cdot (\overline{DBF} \cdot \overline{MFI})] & (9f) \end{aligned}$$

This group of terms allows the interface to become true and produce an eventual \$R, and subsequent interrupt for an Operations Unit operand, in those cases where the Operations Unit already has one or two operands. The assumption is to allow another operand to be sent from memory to the Operations

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.9-52 Sh. No. 9-51

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.1.2 - contd

Unit, because the Operations Unit will be finished with it's current operation by the time the operand arrives.

- 9a) This equation represents the first case: where the Operations Unit has one operand and is not in the process of executing a Repeat Link operation, or the first equations (9c) through (9f) are essentially the inhibit PA cycle of a repeated instruction conditions for the first case.
- 9b) The second case is where the Operations Unit has two operands but a third operand can be sent under certain conditions. Equations (9c) through (9f) still represent the inhibit conditions. The key to this equation is TMCH=2 which indicates that the Operations Unit has two instructions currently being executed. Normally it could be assumed that no other instruction would be allowed until TMCH=0 or 1. However, Z₂₄=SHORT is a register which sets when the first of two instructions sent to the Operations Unit is about to be completed. SHORT indicates that is is a type instruction such as a LDA instruction which requires only a GS, GF cycle in the Operations Unit (see Operations Unit write-up for definitions of the GS and GF cycles.) The assumption is that even though TMCH=2, the interface term may be brought up, because by the time the Control Frame is ready, the short operations unit instruction will have been completed. Other restrictions on this situation are: the instructions currently being processed by the Control Unit may not be Load Registers, any "repeat," or an execute double instruction in the even or odd instruction register (Y or C). If the instruction being processed was any of the above, then the Control Frame could be ready before the Operations Unit was finished.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-53 Sh. No. 9-52

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.1.2 - contd

- 9c) This portion of the equation indicates that the Operation Unit is not in test and step, that all operations are Operations Unit types, that the current instruction is not a store or RAR, or there is not a return instruction or direct operation.
- 9d) When a base frame instruction is being processed, the Control Unit may not proceed until the Operations Unit completes it's operation so BFI inhibits INTR.
- 9e) No multiply or divide operation can take place and no IT modification is allowed. An IT modification may alter a memory location or effect prior conditions within the Operations Unit, so an IT modification is not completed until the Operations Unit is finished with all instructions.
- 9f) If the Direct Buffer in the Base Frame is full and the M-register is full in the Operations Unit, hold up the interface term since the Operations Unit will not be able to accept an operand.

9.3.1.3 Interface Term Inhibits

The previous nine equations define the conditions that cause the interface term to come true and allow the Control Unit to proceed. Seven conditions can inhibit the interface term. These conditions are defined by the state of five flip-flops and two logic levels.

INTR not true = 1 (Refer to 43D163387, sheet 4)

$$\begin{aligned} 1) \text{ PIN flip-flop set} &= \$PIN \cdot (BSIN1B) \\ &\quad + STOP \\ &\quad + ONC \\ &\quad + (WF \cdot \overline{PC} \cdot \overline{MASF}) \\ \text{reset} &= \$INT \cdot (FA + PC) \end{aligned}$$

This flip-flop sets with a \$PIN from the Memory Controller which signals the Processor that the Memory Controller has acknowledged the interrupt and specific command. The enable level (BSIN1B) is a combination of the DPIN flip-flop (for double-precision words and the DPIN) level from the

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-54 Sh. No. 9-53

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.1.3 - contd

Interface Frame. The PIN flip-flop is set with the second \$PIN received from the Memory Controller during double-precision operations. When the PIN flip-flop is set, the indirect word, operand, or external interrupt. The terms STOP, ONC and WF·PC·MASF are to force set the PIN flip-flop for initializing the Processor if an operation is not complete, or if a fault condition is waiting to be serviced.

- 2) D flip-flop set = $\$ \Delta AM2 \cdot \overline{WC}$
reset = $\$ PR + WF$

The D flip-flop is used to inhibit the interface term until the ZI (operation code) bus, and YS- and BS-adders have stabilized. Strobe $\$ \Delta AM2$ sets D about 400 nanoseconds after one of three possible conditions occur which generate it, (see 43D163387, sheet 3).

$$\begin{aligned} \$ \Delta AM2 = & [QIPN1B \text{ (a prestrobe \$IPR for external} \\ & \text{interrupts)} \quad (2a) \\ & + \$C \cdot cSet \text{ P-cycles} \quad (2b) \\ & \cdot [ITS + ITB] \cdot [FAST + FAST] \quad (2c) \end{aligned}$$

- 2a) Strobe QIPN1B is used to generate $\$ \Delta AM2$ any time that the Processor is in a DIS state and a Group VI fault or an external interrupt is detected. Group VI faults are: Timer Runout, Connect and Shutdown. Strobe $\$ \Delta AM2$ is used to set the D flip-flop on the interface term equation to eventually allow the generation of \$C starting the Processor and subsequently servicing of the fault.
- 2b) Any prepare address cycle, except PR, in addition to \$C, will generate $\$ \Delta AM2$.
- 2c) Whenever an ITS or ITB modifier is detected, then the Control Unit must stop address preparation until the second indirect word is brought into the Y or C-register. The term FAST is from the Maintenance Panel for normal CF clock or fast CF clock. FAST and FAST cause $\$ \Delta AM2$ to be speeded up by 18 nanoseconds (FAST) or at normal speed (FAST).

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-55 Sh. No. 9-54

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.1.3 - contd

One additional strobe is generated, as a function of \$ΔAM1 and \$ΔAM2; strobe \$IF. Strobe \$IF is used to start the Interface Frame, and is part of the conditions for generating \$C and \$R, (\$IF·(SAB+SAP)=IFR reset, which stops \$PRC and \$PRII for \$C and \$R). Strobe \$IF can be generated in one of four ways as shown by the terms in the brackets in the following equation for \$IF.

$$\$IF = [QSPEIB \cdot (\overline{DZ}) \cdot ITS + ITB \cdot BZFIOB] \quad (2d)$$

$$BZFIOB = \frac{(FD+FL+FT \cdot OU \text{ stores} \cdot PC \cdot EA)}{}$$

$$\cdot \frac{(ZI = RI \cdot TERM \cdot RR)}{}$$

$$\cdot \frac{(PC)}{}$$

$$\cdot \frac{CT + DIS}{}$$

$$+ [\overline{EIP} \cdot CT \cdot \overline{PC} \cdot TRGO_1 \cdot TMCH=0] \quad (2e)$$

$$+ (FD+FL+FT \cdot OU \text{ stores} \cdot PC \cdot EA) \cdot SDY \quad (2f)$$

$$+ [QSDZ1B (ITS+ITB \cdot BZFIOB)] \quad (2g)$$

- 2d) This equation represents the general case for generating strobe \$IF. All the barred terms represent conditions for which \$IF is inhibited: no Z-function, ITS or ITB address modification, repeated Operations Unit stores, interrupts, conditional transfers, or Processor in a DIS state.
- 2e) This group of terms are for the generation of \$IF during transfers. The Operations Unit must be finished and no interrupt present before allowing \$IF. Level $\overline{EIP}$ is used to inhibit starting \$IF until some of the decodes involved have settled.
- 2f) Strobe \$IF is regenerated concurrent with SDY for completing a sequence of repeated Operations Unit stores, that had been interrupted.
- 2g) When the Z-function level disappears, indicating that Operations Unit registers are now available for operand address preparation designated by the instruction tag the DZ flip-flop is reset. Resetting is accomplished by \$LAST from the Operations Unit generating a \$DOWN which resets DZ. When DZ is reset a pulse is generated which regenerates \$IF.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-56 Sh. No. 9-55

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.1.3 - contd

- 3) SPC flip-flop set = PC
reset = $\$CA \cdot WC$
+ (TERM) + (WF·FAULT)
+ HLT

This flag when set indicates that the Processor is preparing an execute interrupt cycle to service an external interrupt. SPC is reset with a $\$CA \cdot WC$ generated as a result of the execute interrupt information coming from memory during a wait for execute cycle. Resetting of SPC is also accomplished whenever the Processor is servicing a fault or terminate condition.

- 4) DZ flip-flop set = $Z \cdot \$\Delta AM_1$
reset = $\$DOWN\Delta$

This flag when set indicates that the Processor is waiting for a Z-function condition to be cleared. As soon as it is cleared INTR is enabled.

- 5) WI_1 flip-flop

This flag indicates that an instruction pair will be loaded into the Y- and C-registers. As soon as they are loaded, WI_1 is reset and INTR is enabled.

- 6) $(CU/OU \text{ OLAPOFF} + \text{TERM} + \text{BFLAOB}) \cdot \overline{\text{TST} \cdot \text{TMCH}} = 0$

The terms are for control of the interface term from the Maintenance Panel. When the CU/OU OVERLAP OFF switch is on, and the Processor is in a test and step mode, then the interface term is held off until $\text{TMCH} = 0$. For cases where the TMCH counter will not go to zero (Operations Unit faults), BFLAOB enables the interface term.

- 7) $(\text{BWF} \cdot WI_2)$

This level holds off INTR if the CU is handling an ADBn or LDCF with DU modification until after the I Buffer has been filled.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-57 Sh. No. 9-56

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.1.4 Timing Diagram

Figure 9.3.1.4 is a general timing diagram of the important strobes within the Control Unit. The times shown represent the best case times with a one microsecond memory using \$C as a reference.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-58 Sh. No. 9-57

TITLE: ENGINEERING PRODUCT SPECIFICATION

GE-645 PROTOTYPE PROCESSOR

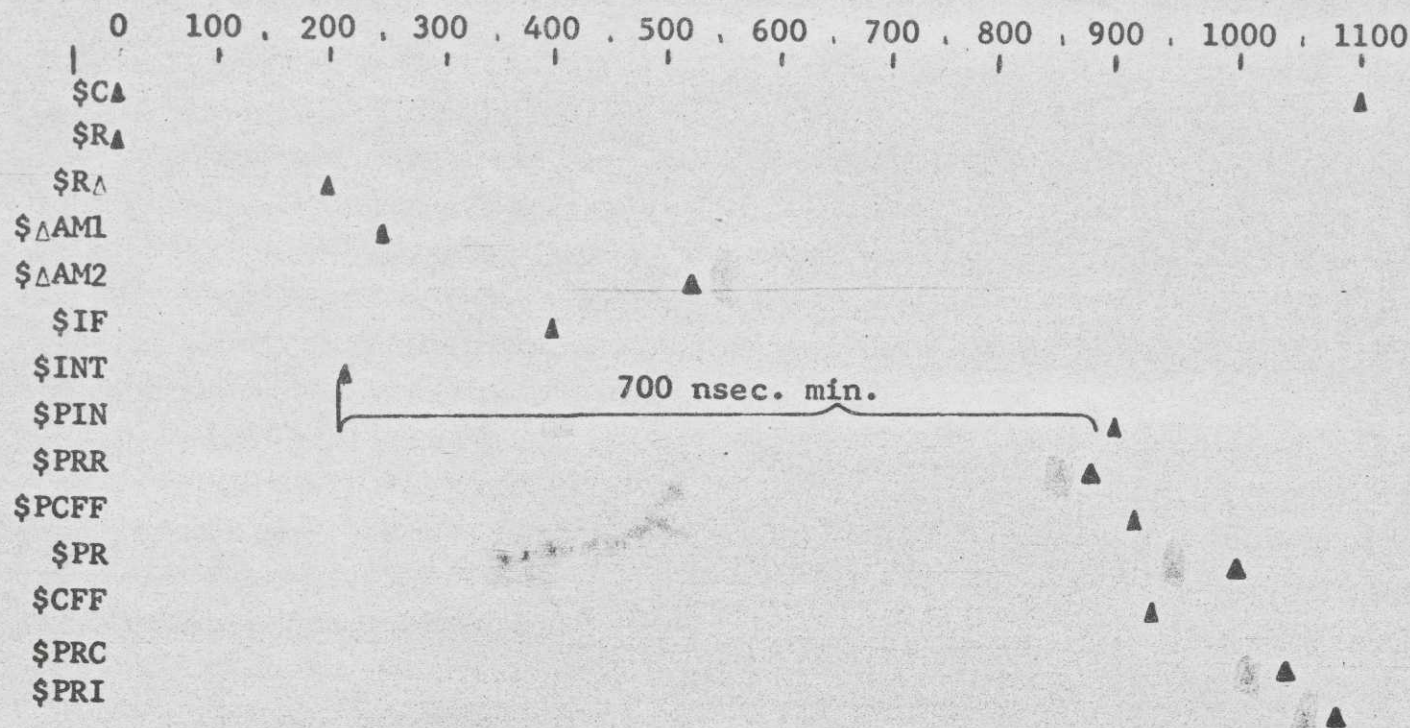


Figure 9.3.1.4 Major Control Unit Strokes, Timing Diagram

- NOTES:
- 1) Times shown are for a one-microsecond memory
 - 2) Processor is assumed to be initialized and is in a DIS state before starting a LDA, LDA, LDA, STA instruction sequence.
 - 3) Processor is in Absolute mode with no address modification.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-59 Sh. No. 9-58

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.2 SEQUENCE CONTROL FLAGS

As mentioned previously in paragraph 9.2.1, the timing sequences within the Control Frame are determined by a number of sequence control flags. The conditions for changing the state of these flags is explained below.

9.3.2.1 Prepare Instruction (PI) (See 43D163387, sheet 31)

The PI flag set and reset equation shown below will be explained term by term. The PI flag is set as a function of \$C and cSet PI, and initialized by WF any time that a fault is about to be serviced.

$$\begin{aligned} \text{cSet PI} &= \text{BSPJ1B} \cdot \overline{\text{DIS}} \cdot \overline{\text{PC}} & (1) \\ \text{BSPJ1B} &= \text{PA} \cdot \overline{\text{TRGO}}_1 \cdot \text{CT} \cdot \text{IC} \cdot \overline{\text{LSI}} \cdot \text{TXI} & (2) \\ &+ \text{PI} \cdot \text{SPI} & (3) \\ &+ \frac{\text{IC} \cdot \text{EA} \cdot \text{cSet RT} \cdot \overline{\text{LSI}} \cdot \overline{\text{TXI}} \cdot (\text{XED} + \text{XEC} + \text{RCU} + \text{TERM} + \text{FD} + \text{FT} + \text{FL} + (\text{LREG} + \text{SREG}) \cdot \text{EA} \cdot \text{CT} = 3)}{\text{TRGO}_1 \cdot \text{EA}} & (4) \\ &+ \text{TRGO}_1 \cdot \text{EA} & (5) \\ &+ \text{RCU} \cdot \text{EA} \cdot \text{ICTA}_{10} & (6) \\ &+ \overline{\text{LSI}} \cdot (\overline{\text{LREG}} \cdot \text{cReset MSLF}) \cdot \overline{\text{IC}} \cdot \text{EA} & (7) \end{aligned}$$

$\overline{\text{cSet PI}}$ = when any of the terms in the above combined equation causes cSet PI to become false.

The meaning of each group of terms is as follows:

- 1) The Processor is not in a DIS (wait for interrupt) state or in the prepare cycle for an external interrupt.
- 2) In the PA cycle of a conditional transfer that is not going to transfer in the odd instruction register, and there is no load-store instruction combination or transfer in the I-register that would preclude going into a PI cycle to fetch a pair of instructions.
- 3) In a PI cycle and must have a second PI cycle & (usually when doing a four-instruction fetch).
- 4) This equation represents the general case for going into PI; when finished with the odd instruction of a pair, pull another instruction pair to fill

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-60 Sh. No. 9-59

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.2.1 - contd

the I-register as the I-register is moved to the Y- and C-working registers. The inhibit terms prevent going into PI for a RPT, RPD, RPL, RET, XEC or XED instruction, or a load-store instruction sequence or transfer instruction in the I-register.

- 5) A satisfied transfer with an effective address requires going into a PI cycle to pull new instructions to fill the I buffer.
- 6) These terms are for an RCU instruction which may change the state of the PI flip-flop to restore it to the condition it was when saved by a previous SCU instruction.
- 7) There was a load-store instruction combination in the I-register and the effective address for the instruction in the Y-register is available. This indicates that two instructions may be fetched to fill the I-register between the execution of the load instruction in the Y-register and the store instruction in the C-register.

9.3.2.2 Prepare Address (PA) (See 43D163387, sheet 31)

The PA flag set and reset equations are a bit complex and will be explained term by term. Set and reset terms on the equation are the same. If the combined equation produces a true output, the PA flag is set on the next SC received; when false, the flag is reset.

$$\begin{aligned} \text{c Set PA} &= \text{BSPA1B} \\ \text{BSPA1B} &= (\text{BSPC1B} \cdot \text{BSPD1B}) + (\text{WF} \cdot \overline{\text{PC}}) \\ \text{BSPD1B} &= (\text{RPD} \cdot \overline{\text{DIS}}) + \text{PI} & (1) \\ \text{BSPC1B} &= \text{BSPE1B} \cdot \text{STOP} \cdot \overline{\text{TRGO}_1} \cdot \text{PI} \cdot \overline{\text{PC}} & (2) \\ \text{BSPE1B} &= [\text{CT} \cdot \text{IC}] & (3) \\ &+ [\text{EA} \cdot \overline{\text{IC}} \cdot \overline{\text{FL}} \cdot \overline{\text{LSI}} \cdot \overline{\text{XED}} + \overline{\text{XEC}} \cdot \text{RCU}] & (4) \\ &+ [\text{LSI} \cdot \text{IC} \cdot \text{EA}] & (5) \\ &+ [\text{TXI} \cdot \text{EA}] & (6) \\ &+ [\text{W} \cdot \overline{\text{FL}}] & (7) \\ &+ [\text{FT} \cdot \overline{\text{TERM}} \cdot \text{EA}] & (8) \\ &+ [\text{EA} \cdot \overline{\text{FD}} \cdot \overline{\text{TERM}}] & (9) \\ &+ [\overline{\text{IC}} \cdot \text{EA} \cdot \overline{\text{FL}} \cdot \overline{\text{TERM}}] & (10) \end{aligned}$$

COMPANY CONFIDENTIAL

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-61 Sh. No. 9-60

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.2.2 - contd

- + [IC·RDE] (11)
- + [(LREG+SREG)·EA·CT = 3] (12)
- + [RCU·EA·ICTA₉] (13)
- + [WI₁·(XEC+XED)] (14)
- + [PI·SPI·(XDE + TRGO₁)] (15)
- + [WC] (16)

ç Set PA = When any one of the terms in the above combined equation causes çSet PA to become false.

- 1&2) Currently in the prepare instruction address cycle for any instruction but a RPD or DIS, the Processor is not stopped, not a satisfied conditional transfer, and not an execute interrupt cycle for an external interrupt.
- 3) A conditional transfer in the odd instruction register.
 - 4) An effective address exists for the instruction in the even instruction register. This instruction is not an RPL, XED, XEC, or RCU and there is no load-store instruction combination in the I-register.
 - 5) An effective address exists for the instruction in the odd location and there is a load-store instruction combination in the I-register.
 - 6) There is a transfer instruction in the I-register and an effective address exists for the current instruction in the working registers.
 - 7) Waiting for the operand from memory for an instruction being repeated under Operation Unit control of a RPL.
 - 8) An effective address exists for an instruction being repeated under control of a RPT and no terminate condition exists.

COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh.9-62 Sh. No.9-61

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.2.2 - contd

- 9) An effective address exists for an instruction being repeated under control of a RPD and no terminate condition exists.
- 10) An effective address exists for an instruction being repeated under control of a RPL that is about to terminate, and it is in the even instruction register.
- 11) Working on the instruction in the odd instruction register but remember that a PI cycle was just completed for an XED instruction in the even instruction register.
- 12) Executing a LREG or SREG instruction except the last cycle.
- 13) An RCU instruction is being executed, which is going to restore the PA flag to its former status at the time that a previous fault condition, and subsequent SCU instruction, stored status.
- 14) Waiting for an instruction, or pair of instructions for the Y- and C-register that is the result of an XEC or XED instruction.
- 15) In a PI cycle for a satisfied transfer that was not a second PI cycle or the result of an XED instruction.
- 16) Waiting for the address of an external interrupt.

9.3.2.3 Prepare Address (PZ) (See 43D163387, sheet 35)

The terms for the set and reset of the PZ flag show that this flag is set whenever an RI, or IR modification is specified by the tag field of an instruction word. Setting of the PZ flag takes place with the \$C that takes the Control Frame out of a WN (wait for indirect) cycle. A term for the RCU instruction allows PZ to reflect the state it had when stored by a previous SCU instruction.

For the indirect word for an instruction being repeated under control of RPL or RPD.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-63 Sh. No. 9-62

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.2.4 Prepare Return or Repeat Indirect (PN) (See 43D163387, sheet 35)

The PN flag is set under the following conditions as can be seen from the logic diagram:

- 1) When an effective address for a RTD instruction is present and no interrupt is present.
- 2) For a RET instruction with no interrupt present.
- 3) Waiting for the indirect word for an instruction being repeated under control of RPT or RPD.
- 4) Restoration of the state of the PN flag by an RCU instruction.
- 5) Whenever there is a fault on a "repeated" (RPT, RPD, RPL) instruction and the Control Frame must go into a PN cycle to terminate the "repeat."

9.3.2.5 Prepare IT Operand (PT) (See 43D163387, sheet 35)

The PT flag is set by the \$C that takes the Control Frame out of the WN cycle; provided that an IT modifier was specified in the instruction or indirect word tag that designated I, or CI address modification; no RPT or RPD instructions being processed, and no interrupt present. The terms for the RCU instruction, as with the other important flags, effect the state of the PT flag depending on what was stored by a previous SCU instruction. The PT flag may also be enabled when in a PR cycle, since the normal sequence of prepare cycles for instructions with IT modifiers that cause a read-alter-rewrite command to the memory is PA → PR → PT.

9.3.2.6 Prepare Rewrite (PR) (See 43D163387, sheet 35)

The PR flag is set concurrently with the \$C that ends a WN cycle for an indirect then tally word, where address modification involving a read-alter-rewrite memory cycle is required. Whenever the PR flag is set, the PT flag will be set on the next \$C. However, PT set does not imply that PR was set. The IT modifications I, CI, ITS and ITB will not cause PR to set.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-64 Sh. No. 9-63

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.2.7 Prepare Execute Interrupt (PC) (43D163387, sheet 21)

PC is a level from any one of the eight flip-flops associated with the Interrupt Present Register (IPR). The IPR is covered in detail in paragraph 9.3.3.

9.3.2.8 Wait for Operand (W) (See 43D163387, sheet 33)

The W flag is set and reset as a function of the following equations:

$$W \text{ set} = BWCFLB \cdot \$PIN$$

$$BWCFLB = (RCU \cdot GBO \cdot INC = 2) + PWA + (RTD \cdot GBO \cdot INC = 0) \quad (1)$$

where PW (43D163387, sheet 32) is the Pre-W flip-flop and is set by:

$$\begin{aligned} PW_{\text{set}} &= \overline{c} \text{Set } PW \cdot \$R \\ \overline{c} \text{Set } PW &= \overline{T} \cdot EA \cdot \overline{TERM} \cdot \overline{RSW} \cdot \overline{Y} \cdot \overline{OVSTINE} \cdot \overline{TRGO}_2 \\ &\quad \overline{OU \text{ STORE}} \cdot \overline{TRGO}_2 \end{aligned} \quad (2)$$

- 1) The terms for RCU and RTD allow W to be set; enabling a strobe \$DRDY to be sent to the Operations Unit so the Indicator Register may be loaded as part of the RCU or RTD instruction execution.
- 2) This equation shows that PW, and subsequently W, will only be set for an Operations Unit operand from memory, since the term $\overline{T}$ is only true for Operations Unit instructions. The terms RSW and $\overline{Y}$ are for direct instructions that do not require memory accesses.

$$W \text{ reset} = \overline{DPFA} \cdot \$DA_2 + WF \quad (3)$$

- 3) Indicates that W will be reset by the first data available pulse for single-precision memory operations and the second data available pulse for double-precision memory operations, or when a fault must be serviced.

COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh. 9-65 Sh. No. 9-64

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.2.9 Wait for Instruction 1 (WI₁) (See 43D163387, sheet 33)

As the equations below for WI₁ show, this flag is only set when fetching instructions to fill the Y- and C-registers. Normally two instructions are fetched and strobed into the I-register, then the contents of the I-register are transferred into the Y- and C-registers. The equations for WI₁ represents only those cases when instructions are fetched (that is, transfers, XEC, XED instructions and store-compare function) for the Y- and C-registers.

$$WI_1 \text{ set} = \$R \cdot BWWI1B$$

$$BWWI1B = \text{cSetXPI} + (PI \cdot XDE) + EA \cdot (XEC + XED) \quad (1)$$

$$\text{cSetXPI} = TRGO_1 \cdot EA + SPI \cdot PI \quad (2)$$

$$SPI = DPI + EXI \cdot \overline{XDE} \quad (3)$$

- 1) Extend the PI cycle (for a second pair of instructions for the T-register and subsequently the Y- and C-registers), or in the PI cycle for an XED instruction in the Y-register (requiring that the Y- and C-registers are to be reloaded) or there is an effective address for an XEC or XED instruction which also require that the Y- and C-registers be reloaded.
- 2) The term cSet XPI is present on any satisfied transfer with an effective address, or when in a PI cycle and a second PI cycle was entered.
- 3) A second PI cycle was entered any time that the base frame fault logic indicates a double PI cycle was accomplished, or a Control Unit store-compare (EX) function came up when no XED instruction was in the Y-register.

Summarizing briefly: The WI₁ flip-flop is set whenever the sequential execution of instructions requires the current and/or remaining instruction in the Y- and C-registers to be repulled from memory because of a transfer, XEC, or XED instruction or the EX (store-compare) function comes true. In addition, when the Processor is initialized and four instructions are fetched, the term DPI (equation 3) comes true from the fault

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-66 Sh. No. 9-65

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.2.9 - contd

logic to cause WI_1 to set thereby allowing the first instruction pair to be strobed into the Y- and C-register directly.

$$\begin{aligned} WI_1 \text{ reset} &= \$DA \cdot \overline{cReset} \cdot WI_1 \\ \overline{cReset} \cdot WI_1 &= \overline{DYC}_\Delta \cdot \overline{DTC}_\Delta + \overline{DYC}_\Delta \cdot DTC_\Delta \end{aligned} \quad (4)$$

- 4) This indicates that WI_1 is reset whenever the data is brought into the Y- or C-register(s).

9.3.2.10 Wait for Instruction 2 (WI_2) (See 43D163387, sheet 33)

The equations for WI_2 represent the general case for a "normal" two instruction fetch: that is, WI_2 is set when waiting for an instruction pair to fill the I-register:

$$WI_2 \text{ set} = \$R \cdot PI \cdot \overline{SPI} \cdot (\overline{XDE} + \overline{TRGO}_1) \quad (1)$$

$$+ RCU \cdot INC = 4 \cdot \overline{ICTA}_0 \cdot \overline{PDP}_\Delta \cdot \$PIN \quad (2)$$

- 1) Any instruction fetch that is not the result of a second PI cycle, XED instruction in the Y-register, or a satisfied transfer.
- 2) Whenever an RCU instruction is recognized, a strobe is generated to set WI_2 if the original state of the PI flag was a "0" during a previous SCU instruction, since the two instructions saved by the SCU instruction must go into the I-register.

$$WI_2 \text{ reset} = \$DA[W_\Delta \cdot \overline{DPF} + \overline{DPS}] + WF + SFF \quad (3)$$

- 3) This means that WI_2 is reset when data is on the lines to the Processor from the memory, that is the second half of a double-precision read-restore operation. (Both instruction words have been received from memory and reside in the I-register). The terms DPF and DPS are for a double-precision fetch and to inhibit the reset of WI_2 during the termination of "repeat" instruction.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-67 Sh. No. 9-66

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.2.11 Wait for Indirect (WN) (See 43D163387, sheet 33)

The WN cycle is entered whenever a previous PA, PT or PZ cycle does not yield an effective address for an operand, and no fault is being serviced.

$$WNset = \$C[(PA+PZ+PT) \cdot \overline{EA} \cdot \overline{WN} \cdot \overline{RR} \cdot \overline{WF} \cdot \overline{SNO}]$$

As the set equation shows, WN is set as soon as the fetch for the indirect word is started. The terms RR, WF and SNO are to prevent the setting of the WN flip-flop for conditions that are going to cause the servicing of a detected fault.

$$WNreset = \$DA_2 \cdot \overline{creset} WI_1 + WF$$

As the reset equation shows, WN is reset when data from memory is available to be strobed into the Y-or C-register. Level creset WI₁ is high when data is to be brought into the Y- or C-registers. Whenever WF is present WN is forced reset.

9.3.2.12 Even/Odd Sequence (ICF, ICG) (See 43D163387, sheet 30)

The conditions for resetting and setting the IC (F,G) flag are shown in the equation below. Reset conditions are shown first since the Y-register (even instruction) is normally serviced before the C-register (odd instruction). IC (F,G) consists of two flip-flops due to loading requirements but with identical inputs.

$$\underline{IC (F,G) reset} = \$C \cdot \overline{cReset} IC + PNLSW/ZDIRF$$

$$\overline{cReset} IC = [TXI \cdot IC \quad (1)$$

$$+ LSI \cdot EA \cdot IC \quad (2)$$

$$+ EA \cdot IC \cdot \overline{FD} \cdot \overline{TERM} \quad (3)$$

$$+ RCU \cdot EA \cdot \overline{ICTA}_5 \quad (4)$$

$$+ \overline{LSI} \cdot \overline{ICTB}_{17} \cdot \overline{PI} \cdot \overline{SPI} (\overline{XDE} + \overline{TRGO}_1) \quad (5)$$

$$+ WI_1 \Delta \cdot \overline{XED}] \cdot \overline{RDE} \cdot \overline{WF} \quad (6)$$

- 1) There is an unconditional transfer in the I-register and the Control Frame is currently working on the odd instruction in the C-register.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-68 Sh. No. 9-67

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.2.12 -contd

- 2) There is a load-stroe instruction in the I-register and an effective address exists for the instruction in the C-register.
- 3) The Control Frame has finished with the second instruction of the two instructions designated by an RPD instruction but has not terminated the RPD instruction sequence.
- 4) An RCU instruction is being executed which will restore the status of the IC (F,G) flag to a reset condition.
- 5) This group of terms represent the general case for resetting the IC (F,G) flag for the even instruction.
- 6) Waiting for the instruction pair designated by an XED instruction to come from memory. RDE and WF prevent the reset of IC (F,G). There was no XED instruction in the even instruction register. Had there been an XED instruction, IC must not change because the instructions being fetched as a result of the XED instruction, will come into the Y- and C-registers and the instruction in the Y-register will be prepared first. If the Processor is waiting to start a fault sequence IC (F,G) is not changed.

The conditions for setting IC (F,G) are as follows:

$$\begin{aligned} \text{IC (F,G) set} &= \$C \cdot c\text{Set IC} & (7) \\ c\text{Set IC} &= \{ [(\overline{\text{LDR}} + \text{STR}) \cdot \text{EA} \cdot \text{CT} = 3 & (7a) \\ &\quad \cdot \overline{\text{DIS}} & (7b) \\ &\quad \cdot \overline{\text{RPD}} & (7c) \\ &\quad \cdot c\text{Set RT} & (7d) \\ &\quad \cdot \text{STOP} \cdot \text{TRGO}_1 & (7e) \\ &\quad \cdot (\overline{\text{LSI}}) \cdot [\text{CT} \cdot \overline{\text{IC}} + \text{EA} \cdot \overline{\text{IC}} (\text{TERM} + \overline{\text{FL}} + \text{FT})]] & (7f) \\ &\quad + [\text{LSI} \cdot \text{PI} \cdot \overline{\text{SPI}}] & (8) \\ &\quad + [\text{RCU} \cdot \text{EA} \cdot \text{ICTA}_5] & (9) \\ &\quad + [\overline{\text{IC}} \cdot \text{ICTB}_{17} \cdot \text{PI} \cdot \overline{\text{SPI}} (\overline{\text{XDE}} + \text{TRGO}_1)] & (10) \\ &\quad \cdot \overline{\text{WF}} & (11) \end{aligned}$$

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-69 Sh. No. 9-68

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.2.12 - contd

- 7) The terms in this equation are the inhibits for those conditions where IC (F,G) is not to be set.
- 7a) Not doing a LREG or SREG instruction that is not complete.
- 7b) Not in a DIS state waiting for an external interrupt.
- 7c) Not currently preparing an RPD instruction in the even instruction location (RPD in the instruction register is not allowed).
- 7d) Not doing a RET or RTD instruction.
- 7e) The Processor is not stopped or recognizing a transfer.
- 7f) There is no load-store instruction combination in the I-register, no conditional transfer in the Y-register and an effective address and terminate condition exists for a RPT, RPD, RPL instruction in the Y-register; or an effective address exists for the instruction in the Y-register, and this instruction is not RPT or RPL.
- 8) The Control Frame is finishing a PI cycle that is not the second PI and there is a load-store instruction combination in the I-register.
- 9) An RCU instruction is being executed which may effect the setting of IC.
- 10) This equation represents the case for setting IC (F,G) for an odd instruction that if fetched in to the C-register.
- 11) Whenever a fault condition is about to be serviced IC (F,G) is not changed.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-70 Sh. No. 9-69

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.3 INTERRUPT PRESENT REGISTER (IPR) (See 43D163387, sheet 21)

The IPR is an eight-bit register, each bit of which corresponds to one of the eight (numbered 0-7) "ports" on the Processor. Each individual stage of the IPR is set as a function of an interrupt present from one of the ports connected to a Memory Controller, and a \$C which initiates a PA, PZ, PN or PT address preparation cycle. When the Processor is in a DIS (delay until interrupt) state, the presence of an interrupt causes one of the stages of the IPR to be set for the port which causes the interrupt. Setting of one of the IPR stages causes a level designated PC to be generated which, when recognized by the fault logic, places the Processor in a prepare execute interrupt state.

9.3.3.1 Interrupt Sampling

Sampling of the interrupt present lines for each Processor port is accomplished with a \$IPR which sets any stage (IPR₀₋₇) which has its interrupt present line (IP₀₋₇) high. Strobe \$IPR is generated by a \$C when the Processor is running and bit 2 of the current instruction a "0," by an interrupt present at one of the Processor ports when in the DIS state, by a Group VI Fault (Connect, Timer Runout, Shutdown), or by a Execute Fault set as a function of some of the Maintenance Panel switches.

$$\begin{aligned} \$IPR \text{ (Processor running)} &= \$C \cdot \overline{MLS F} \cdot (PA + PZ + PN + PT) \quad (1) \\ &\quad \cdot (MSY \cdot C28 \cdot IC) + (MSY \cdot Y28 \cdot \overline{IC}) \end{aligned}$$

- 1) Strobe \$IPR is generated approximately 120 nanoseconds after the start of any PA, PZ, PN or PT address preparation cycle unless the instruction presently being executed has its interrupt inhibit bit set to a "1," or is a multiple operations unit cycle instruction (LREG, SREG, etc.).

$$\begin{aligned} \$IPR \text{ (Processor in DIS state)} \\ &= (IP0 + IP1 + \dots + IP7 + FRQ) \cdot DIS \cdot \overline{PA} (\overline{SPC} + \overline{SRF}) \cdot \overline{PI} \quad (2) \end{aligned}$$

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-71 Sh. No. 9-70

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.3.1 - contd

- 2) Strobe \$IPR is generated whenever an interrupt present line is high from one of the eight memory ports or a Connect, Timer Runout or Shutdown Fault is detected. The term PA is to prevent interrupting if in the PA cycle of a DIS instruction rather than the Processor waiting in a DIS state. Both SPC and SRF in addition to PI, are used to inhibit the generation of \$IPR during certain areas of critical timing which could possibly allow \$IPR during PI.

9.3.3.2 Reset Conditions

Resetting of the IPR is normally done whenever a \$INT is sent to memory in response to an external interrupt, and when in a PC cycle. Strobe \$IF is for cases where there will be no \$INT issued as a result of a previous execute interrupt cycle.

If a terminate or stop-for-fault condition occurs, then the IPR is forced to reset and inhibit recognizing any interrupts until the particular condition (TERM+WF·SFF) serviced.

9.3.4 INPUT DATA CONTROL AND STROBE GENERATION FOR THE Y-C- AND I-REGISTERS

Bringing in data, in the form of instructions, to the Y-, C- and I-registers and how this data should be strobed into the effected registers is rather complex because of the four instruction look-ahead feature in the Control Frame. Generally speaking, the actions and conditions required to bring data into the Y-, C- and I-registers, fall into the following areas:

- 1) Control of the V (data-in) switch to control the data to the Y-, C- and I-register. Control of the VTA, VTB and TIC switches for data to the Y- and/or C-registers. Instructions can be brought in as a result of:
 - a) A normal two- or four-instruction fetch.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-72 Sh. No. 9-71

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.4 - contd

- b) Address modification on the instruction currently being processed.
 - c) Instructions which restore the Control Frame to some previous state (RTD, RCU).
 - d) Executing instructions which cause a repulling of new instructions, or a transfer of control (XEC, XED instructions and all satisfied transfers).
 - e) Fault conditions which cause a "snapshot" to be taken (the Y- and C-registers contents are strobed into the I-register prior to servicing the fault which caused the "snapshot").
- 2) Generation of strobe \$YOC which is used to generate the actual strobes to strobe the Y- and C-registers. Strobe \$YOC can be generated because of:
- a) A "normal" instruction fetch resulting in instructions coming into the Y- or C-registers via the I-buffer or V-switch.
 - b) The ADB_n, LDCF, or RTD base instructions being executed.
 - c) Address modifications involving a read-alter-rewrite memory cycle (AD, SD, DI, DIC etc.)
 - d) An XEC or XED instruction in the Y- or C-register respectively, which will cause their contents to be replaced or restored.
- 3) Control of the strobes to the address, operation code (including bits up to bit 29), and tag portions of the instruction word that is brought in the Y and/or C-registers. The strobes being generated by \$YOC.
- 4) Generation of strobes \$ZIE and \$ZIO to load the I-register whenever instructions are being brought in from memory as indicated by the condition of the WI₂ flag.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-73 Sh. No. 9-72

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.4 - contd

The four general conditions for control of data in the form of instructions to the Y-, C-, and I-registers and the resultant strobes generated will be examined in detail via the applicable equations.

9.3.4.1 Data-In-Control (See 43D163387, sheet 26)

There are eight control points that control the selection of data to the Y-, C- and I-registers: VTA, VTB (Y- and C-register); DTV (turn on ZDI_{0-29} for data from memory); BTTVOB (turn on ZDI_{30-35} for data from memory); BTB (turn on BS_{0-17} for instructions or address modification requiring the contents of the BS-adder); TIC for transferring data from the I- to Y- and C-registers; SNO, SNI for transferring the Y- and C-registers to the I-register during the "snapshot" sequence for a fault. (Examine 43D160212 sheet 5 to see the relationship of the control points to data being brought into the Y-, C-, and I-registers.)

$$\begin{aligned}
 VTA &= [WF] & (1) \\
 &+ [\overline{ADB_n} + LDCF] \overline{CSR} \cdot \overline{IC} \cdot (DU+DL) \cdot \overline{CFR} \cdot \overline{WI_2} & (2) \\
 &+ [PR \cdot (SCR \cdot SD \cdot DI \cdot DIC) \cdot \overline{IC}] & (3) \\
 &+ [DTC \cdot \overline{DYC} \cdot \overline{WN} \cdot \overline{IC}] & (4) \\
 &+ [DYC \cdot BBVA1B] & (5) \\
 BBVA1B &= XED & (5a) \\
 &+ \overline{WC} \cdot \overline{WF} & (5b) \\
 &+ \overline{ICTB_{17}} \cdot XPI & (5c) \\
 &+ \overline{IC} \cdot BYEJ1B & (5d) \\
 BYEJ1B &= XEC & (5d-1) \\
 &+ (\overline{XEC} + XED) \cdot RDE & (5d-2) \\
 &+ \overline{WN} & (5d-3) \\
 &+ \overline{FL} \cdot \overline{RDE} \cdot \overline{TERM} & (5d-4) \\
 &+ \overline{RET} \cdot \overline{RT} & (5d-5) \\
 &+ \overline{DYC} \cdot \overline{IFR} \cdot \overline{GBO} \cdot \overline{ADB_n} + LDCF + \overline{RTD} & (5d-6)
 \end{aligned}$$

- 1) Waiting for a fault condition where an XED instruction will be "brute-forced" into the Y-register.
- 2) Executing an ADB_n or LDCF instruction with bits 0-17 of the instruction word interpreted as direct

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-74 Sh. No. 9-73

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.4.1 - contd

operand, but not an OU operand since the execution of the ADB_n and LDCF instructions take place in the Base and Control Frames. Had DU or DL address modification not been specified by the instruction word, a memory access would have to be made and the VTA level brought up for the "normal" case of data to the Y-or C-registers. (See equation 19 for details). CFR and WI_2 hold off the control until the operand is on the data in lines.

- 3) During the rewrite portion of a read-alter-rewrite memory cycle for the modifiers shown, the address portion of the indirect then tally word must be changed to the new modified address, prior to fetching an operand.
- 4) During ITS or ITB the second word of the indirect pair must be brought into the Y- or C-register. This equation accomplishes this.
- 5) Level DYC_A is the data to Y- or C-register flip-flop which is discussed in the next paragraph under strobe $\$YOC$ generation.
- 5a) An XED instruction is being executed which will bring in two new instructions to replace the ones currently in the Y- and C-registers.
- 5b) The Control Frame is in the wait cycle of an execute interrupt and is waiting for the interrupt block address to come back from the highest unmasked interrupt cell in the memory controller. Level WF is to ensure that the previous "snapshot" and fault sequence is complete before entering WC .
- 5c) The first pair of instructions for a four-instruction fetch is about to come into the I-register and the Y-register must be loaded with the even instruction word.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-75 Sh. No. 9-74

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.4.1 - contd

- 5d-1) Executing an XEC instruction which required pulling a new instruction into the Y-register.
- 5d-2) Repulling the old instruction that formally occupied the C-register but was lost due to an XED instruction in the Y-register. An XEC or XED instruction is not allowed as the first instruction of a pair of instructions specified by previous XEC or XED. Notice that the instruction coming in will come into the C-register via VTB as indicated by RDE and the fact that IC is set for this condition (see equation 7 of paragraph 9.3.2.11).
- 5d-3) Waiting for an indirect word from memory.
- 5d-4) Executing the repeated instruction specified originally by an RPL instruction, no terminate condition has been detected, and the repeated instruction was not an XED in the even instruction location.
- 5d-5) Executing a RET or RTD instruction when in a general base operation state (RT contains RTD.GBO).
- 5d-6) During ADB₀ or LDCF or RTD the operand is brought into the Y- or C-register and then added to or sent to the proper register in the Base Frame.

The equations for VTB are the same as VTA except that IC takes the place of IC, ICTB₁₇ takes the place of ICTB₁₇, and the equation of (5) does not contain XED (5a), because an XED is not allowed in the odd instruction location (C-register).

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-76 Sh. No. 9-75

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.4.1 - contd

$$\begin{aligned} \text{DTV (turn on ZDI}_{0-29}) &= \text{BBVPIB} & (6) \\ &+ \text{BDVTOB} & (7) \\ &+ \text{RCU.GBO} & (8) \\ &+ \text{PR.AD} & (9) \\ &+ \text{WI}_2 & (10) \end{aligned}$$

6&7) These equations are the same as (5) above and depend on whether the Y- or C-register must be loaded.

8) Execution of an RCU instruction and restoring the Control Frame status that was stored by a previous SCU instruction.

9) Performing an IT type AD address modification, where the delta portion of the IT word from memory must be on the ZDI lines to be added to the operand address in the YS-adder (DTV will in turn allow BTTVOB and ZDI₃₀₋₃₅).

10) In the normal wait period for an instruction pair to come from memory to fill the I-register

$$\begin{aligned} \text{BTTVOB} &= \text{DTV} & (11) \\ &+ \text{PR.SD} & (12) \end{aligned}$$

11) Any time ZDI₀₋₂₉ is turned on as a result of the previous condition shown in equations 1-10, all 36 bits on ZDI must be present.

12) During IT type SD address modification, only the delta portion of the indirect then tally word is necessary to form the new operand address that is rewritten into memory during the PR cycle.

BTV (BS₀₋₁₇ to ZDI) = Equation (2), (3) and (4) above (keeping in mind that IC differs for VTA and VTB). The BS-adder is switched to the input of the Y- and C-register via the VTA, VTB switches during the PR cycle for indirect then tally address modification. At the end of the PR cycle the new modified address is strobed into the Y- or C-register in preparation for the final operand address cycle.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.9-77 Sh. No. 9-76

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.4.1 - contd

TIC (Transfer I to the Y- and C-registers, see 43D163387
sheet 24) = [TXI (13)
+ LSI (14)
+ PI · SPI · (XDE + TRGO₁)] (15)
· TIB (16)
· [DYC_Δ + (DTC_Δ (ITS + ITB + WN))] (17)]

- 13) If there is a transfer instruction in the I-register no PI cycle is entered to fetch a new pair of instructions to fill the I-register, so TXI is needed to generate TIC.
- 14) When a load-store instruction combination is in the I-register, a PI cycle is postponed until the time interval between the load and store instruction. LSI allows the I-register to be strobed into the Y- and C-registers without entering a PI cycle.
- 15) This group of terms represent the general case for fetching a pair of instructions to fill the I-register and represents a normal PI cycle for the second fetch of a four instruction fetch.
- 16) If TIB is not set indicating that the contents of the I-register are ready to be transferred, TIC is inhibited.
- 17) If data is to be brought into the Y- or C-register, then the I-register is not to be transferred, and TIC is inhibited.

SNO, SNI (transfer Y- and C-registers to I-register) - These control points are brought up by the fault logic in the Base Frame. Discussion of the conditions that generate SNO, SNI are covered in Section 10.5.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-78 Sh. No. 9-77

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.4.2 Strobe \$YOC Generation (See 43D163387 sheet 24)

Strobe \$YOC is generated any time that data is brought into the Y- or C-register. Control of the strobe, to the various bits of the registers, is covered in the next paragraph. As the equation below shows, generation of \$YOC is possible under three conditions: data coming into the Y- or to C-registers as part of a normal two, or four-instruction fetch; changing of existing data due to instruction or address modifications that involve a read-alter-rewrite memory cycle; anytime an ADB_n or LDCF instruction with a DU or DL (direct operand) modifier is encountered and no fault condition exists:

$$\begin{aligned} \$YOC &= + \$R \\ &+ \$GDA \\ &+ \$DS \cdot PR \\ &+ \$PR \cdot (ADB_n + LDCF) \cdot \overline{CSR} \cdot (DV + DL) \end{aligned} \quad \begin{aligned} (18) \\ (19) \end{aligned}$$

where:

$$\$GDA = \$DA_2 \cdot (DYC_{\Delta 2} + (DTC_{\Delta} \cdot (ITS + ITB + \overline{WN}))) \quad (20)$$

18) The Control Frame has stored the modified data for a read-alter-rewrite memory cycle, that is the result of some IT address modification, into the DOR register in the Interface Frame. Now the final operand address preparation cycle may be entered. Strobe \$YOC is generated because a modified address may be strobed into the applicable instruction register as a result of the specified address modification, and this address used to form the effective address for the operand.

19) If the ADB_n or LDCF instructions have direct operands, then no memory access is required. The adding that takes place in executing ADB_n or LDCF is to the address or control field of the specified address base register(s); the BS-adder does the adding, then BS_{0-17} is sent to the Base Frame. Since the possibility exists for an internal base to be added to the information brought into the BS-adder on a direct operand (if bit 29 of the instruction word is a "1" and an internal base is specified) two operations must be completed:

a) Add the internal base in the BS-adder with the direct operand contained in the instruction word.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-79 Sh. No. 9-78

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.4.2 - contd

- b) For ADB_n , add the specified ABR in the BS-adder with the contents of the direct operand and internal base. For the LDCF instruction the internal base addition effectively destroys the ABR control field information.

Since both the internal base and ABR designated by the instruction are added in the BS-adder (for ADB_n); the intermediate results of the first addition (internal base and direct operand) must be saved in the applicable instruction register (Y or C). Hence, generation of \$YOC in this case. When preparing to enter a fault routine \$YOC is inhibited.

- 20) This group of terms represent the general case for generating a strobe \$YOC for the Y- or C-register during a normal instruction fetch; in cases where an ITS or ITB tag modifier is encountered as a result of address modification; or when the C-register must be loaded independently of the Y-register (XED instruction in Y-register, or XEC instruction in C-register).

In the equation of (20), the terms $DYC_{\Delta 2}$ and DTC_{Δ} indicate when data is to be brought into the Y- or C-registers. Referring to the logic diagram for the inputs to DYC , note that DYC is set any time the Control Frame is waiting for an instruction or indirect word to fill the Y- and/or C-register; specifically:

- a) The operand for the base instructions which are executed within the Control Frame (ADB_n , LDCF, RTD).
- b) Instructions as a result of a WI_1 cycle which is to result in an eventual two-instruction fetch for the Y- and C-registers.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-80 Sh. No. 9-79

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.4.2 - contd

This represents the general case where the I-register is to be strobed into the Y- and C-register as two new instructions are brought into the I-register, or when an indirect word is brought in as a result of address modification.

- c) Any prepare cycle (except PR) which may cause new data to be brought into the Y- or C-register.

An examination of the inputs for DTC shows that DTC is only set if DYC is set. What this indicates is that DYC set is for the first half of a double-precision instruction or indirect word fetch to the Y- or C-register. DTC is for the second half of a double-precision instruction or indirect word (ITS or ITB modification) fetch.

9.3.4.3 Strobe Control for Y- and C-Registers (See 43D163387 sheet 25)

Strobe \$YOC is generated whenever data is brought into the Y- or C-registers as shown in equations (18) through (20). Control of strobe \$YOC to the major portions of the Y- or C-register is divided into three parts: \$ZYE and \$ZYO for bits 0-17; \$ZCE and \$ZCO for bits 18-29; \$ZCF and \$ZCG for bits 30-35. The conditions which control the distribution of the strobe to the Y-register is essentially the same as to the C-register, so only distribution to the Y-register is discussed.

$$\$ZYE_{0-17} = \$YOC \cdot (\overline{EXI} \cdot BYSC1B) \quad (21)$$

$$\begin{aligned} BYSC1B &= VTA \cdot \overline{BVT} + VTA[(SD+DI+DIC+SCR) + (ADB_n + \\ &\quad LDCF \cdot (DU+DC) \cdot CSR)] \quad (21a) \\ &\quad + YOE \quad (21a-1) \\ &\quad + TIC \quad (21a-2) \end{aligned}$$

21) The address field (bits 0-17) is strobed any time data is brought into the Y-register, the store-compare function is not present (Y-register only) and the terms in 21 through 21a-2 are satisfied.

21a) The two groups of terms with VTA are for conditions where the address field of the instruction word is under IT type SD, DI, DIC, or SCR address modification which requires a new updated operand address.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-81 Sh. No. 9-80

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.4.3 - contd

The term $\overline{BVT}$ contains both $\overline{IC}$ and PR in addition to SD, DI, DIC, and SCR, thereby allowing the new modified address of the indirect then tally word to be strobed into Y_{0-17} , and when the operand for a ADB_n or LDCF with DU or DL modification must be strobed into Y.

j 21a-1) The term YOE is for conditions where a store-compare function is detected or a fault condition is being serviced which results in Y_{0-17} being reloaded.

21a-2) TIC represents the general case where the Y-register is going to be loaded from the I-register for the next pair of instructions in sequence.

$$\$ZCE_{18-29} = \$YOC \cdot (\overline{EX_1} \cdot (\overline{IOS} + PI) \cdot BCSY1B) \quad (22)$$

$$BCSY1B = VTA \cdot \overline{BVT} + YOE + TIC \quad (22a)$$

22) This equation shows that the operation code portion of the word that is brought into the Y-register is only strobed when a new instruction is fetched. Terms $\overline{IOS}$ or PI also include provisions for the instructions that, in effect, bring an operand into the Y-register for execution within the Control Frame (instructions ADB_n , RTCD, LDCF, RPL, RPT, RPD, RET). The "repeat" instructions are included since the repeated instruction(s) that is designated, does not have the operation code changed during the repeat process.

22a) This equation represents the general group of conditions for which the operation code is changed when data is brought into the Y-register.

$$\$ZCF_{30-35} = \$YOC \cdot [(\overline{ITS} + PI)(\overline{EX_1})(BCYT1B)] \quad (23)$$

23) The terms for this equation have been explained before with the exception of $\overline{ITS}$. By reference to sheet 26 for the generation of $\overline{ITS}$, note that if a "repeat" or a "return" type is being executed, then $\overline{ITS}$ is generated and strobe $\$ZCF_{30-35}$ is inhibited.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-82 Sh. No. 9-81

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.4.3 - contd

This is because of restrictions on the use of the address modification that can be designated by the tag field of these instructions (RET, RTCD, RPT, RPD, RPL).

Referring back to sheet 25, note that control of the strobes for the C-register is identical to the Y-register except for the term $EX_1 \cdot EX_1$ is required as an inhibit on the Y-register strobes whenever a store-compare (EX) function is generated against the C-register. The C-register must be reloaded by the EX function forcing an XEC instruction to repull the instruction in the C-register. Since EX_1 is required to generate YOE and enable the strobe control to both the Y- and C-registers, EX_1 is required to prevent the Y-register from getting strobed and losing its contents when the C-register is reloaded.

9.3.4.4 Strobe Generation for I-Register (See 43D163387, sheet 33)

Information is strobed into the I-register under two conditions:

- 1) Doing a "snapshot" sequence where the Y- and C-registers are loaded into the I-register in preparation for entering a fault routine.
- 2) Normal instruction fetches during a WI_2 cycle for the two instruction pair.

Strobes \$ZIE, and \$ZIO are generated for the two general conditions shown, as can be seen from the logic diagram.

9.3.5 ICT STROBES AND TRACKING LOGIC FOR ICTC, ICTB, ICTA' AND ICTA INSTRUCTION COUNTERS

The Control Unit contains four instruction counters to hold the address of an instruction during the various stages of address preparation or execution within the Control Unit and when being executed within the Operations or Appending Unit:

ICTB - contains the address of the even instruction of the instruction pair contained in the I-register.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-83 Sh. No. 9-82

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.5 - contd

ICTC - contains the address of the even instruction of the pair of instructions in the Y- and C-registers during the course of a normal instruction/operand address preparation sequence. When the Control Unit is restored as a result of an RCU instruction from a previous fault condition, or if a transfer instruction is encountered, ICTC could contain the address of the odd instruction.

ICTA' - contains the address of the even or odd instruction which in the Y- or C-register is to be sent to the Operations Unit (for operations unit instructions) or executed within the Control or Base Frames (control frame or base frame instructions). When the Control Frame is restored as a result of an RCU instruction from a previous fault condition, ICTA' is used to hold the bits that will restore the various status flags within the Control Frame (with the exception of the "repeat" flags which are restored from the ZDI lines as data is brought from memory).

ICTA - contains the address of the even or odd instruction sent to the Operations Unit for execution (for operation unit instructions) or the address of nonoperations unit instructions executed within the Control and Base Frame.

The data paths between the four ICT counters are shown on 43D160212 sheet 5. Notice that bits 0-16 of ICTB are transferred progressively to ICTC to ICTA' to ICTA. Bit 17 of the ICTA' and ICTA counters may be changed depending on whether a normal instruction sequence for preparation and execution is followed, or a fault of some type occurs. The blocks labelled "V" and "ATA" perform the logical functions to decide whether bit 17 of ICTA' and ICTA should be "0" or "1." Generally speaking, the ICT tracking falls into three distinct categories:

- 1) Cases where instructions are being fetched, prepared, and executed in a normal fashion (in sequence, no transfers, faults, etc.).'

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-84 Sh. No. 9-83

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.5 - contd

- 2) Cases where a fault is detected and the ICTC register must be saved for nonoperations unit (except for parity) faults, or ICTA saved for operations unit faults, and parity faults for nonoperation unit instructions.
- 3) When an RCU instruction is encountered to restore the status of the Processor, certain of the words specified by the RCU instruction are used to reset or set the Control Frame flags from ICTA' and restore the ICTC counter.

The three different modes are illustrated in Fig. 9.3.5.5 and the logic diagram is 43D163387, sheet 14.

9.3.5.1 Normal ICT Tracking

Normally, instructions are fetched in pairs by switching the ICTB register to the YS-adder input adding +1 in both the YS- and BS-adders and fetching a pair of instructions for the I-register.

(Refer back to the paragraph and flowchart on instruction fetches for details.) When a \$R is generated to produce an interrupt to memory for the pair of instructions for the I-register, ICTB₀₋₁₇ is strobed with the address of the instruction pair still contained in the BS-adder. The same process is repeated for another instruction pair, the instructions in the I-register are moved to the Y- and C-registers, and ICTC₀₋₁₇ is strobed with the contents of ICTB₀₋₁₇. Address preparation is then started for the instruction in the Y-register.

When the instruction in the Y-register is ready for execution, and it is an operations unit instruction, the operation code is stored in the RE buffer within the Control Frame until the Operations Unit can accept it. Concurrent with saving the operation code in the RE buffer, a strobe \$ZOR that strobes the RE buffer transfers ICTB₀₋₁₆ to ICTA' ₀₋₁₆. Bit 17 of ICTA' is set

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

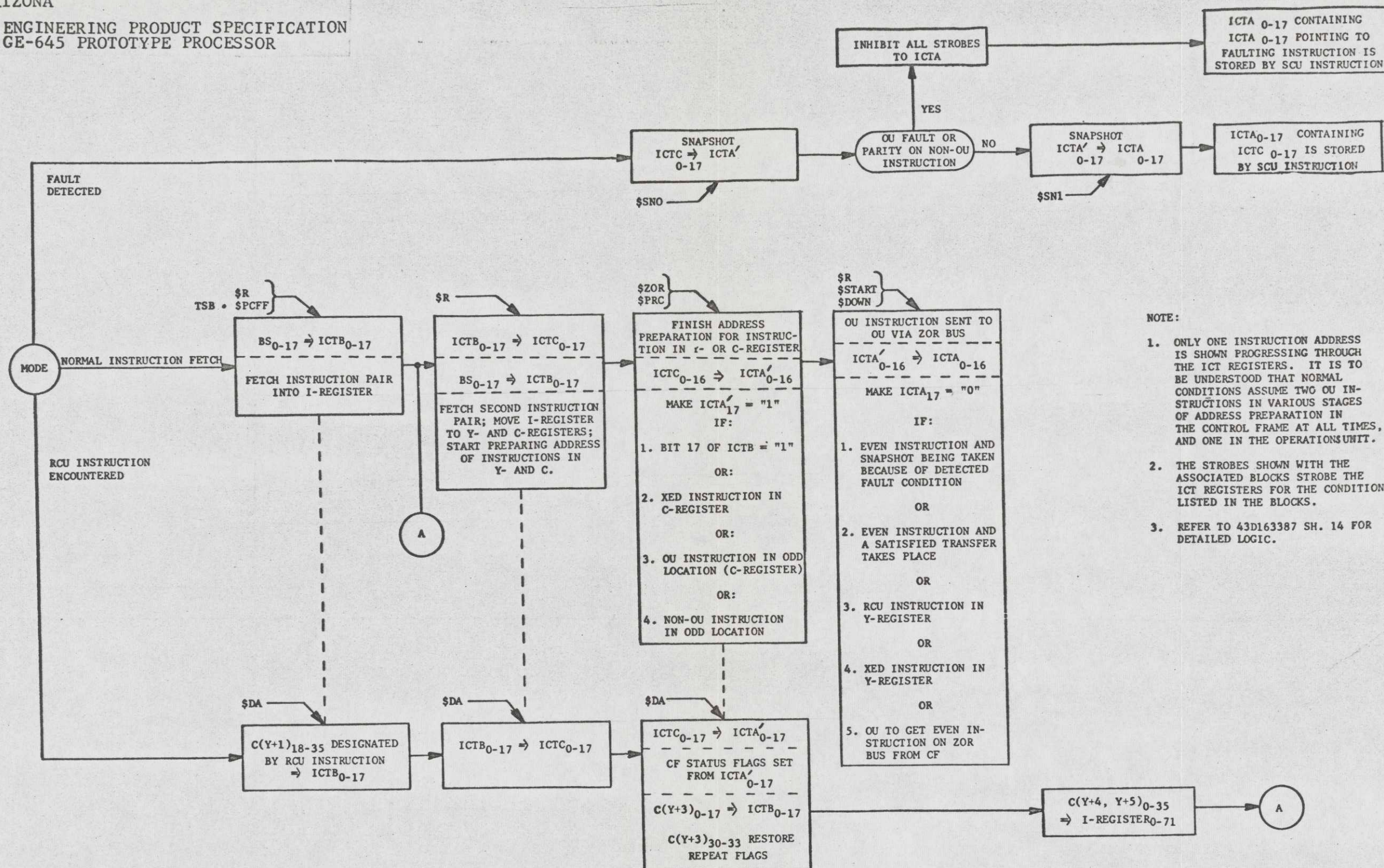


FIG. 9.3.5 GENERALIZED ICT TRACKING, FLOWCHART

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-86 Sh. No. 9-85

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.5.1 - contd

to a "1" or remains a "0" for those conditions as shown on Fig. 9.3.5. For the particular case we are discussing $ICTA'_{17} = "0."$

When the Operations Unit is ready to accept the operation code and begin executing the instruction, a strobe \$START is generated and $ICTA'_{0-16}$ is transferred to $ICTA_{0-16}$. Bit 17 of $ICTA$ will be a "0" because of the conditions shown on Fig. 9.3.5. This process is repeated as long as operations unit instructions are being fetched, prepared and executed in the normal manner. The timing between the various strobes varies greatly with the instructions fetched, operand address modification, execution, etc. The tracking of bit 17 when transferring an operations unit instruction address from $ICTA'$ to $ICTA$ is controlled by the B' flip-flop shown on sheet 14. This flip-flop is only set when the Operations Unit is ready to accept an instruction not when it is put on the ZOR bus to the Operations Unit. In a sense, the B' flip-flop tracks the B control flip-flop for the ZOR bus switching of the RE, RO buffers to the Operations Unit.

For nonoperations unit instructions, $ICTA'$ and $ICTA$ tracking is the same except that the address is transferred from $ICTC$ to $ICTA'$ by \$PRC and from $ICTA'$ to $ICTA$ by \$R; \$R to $ICTA$ implying that the nonoperations unit instructions have already been executed.

9.3.5.2 Fault Detected Tracking

If a fault condition is detected by the processor fault logic in the Base Frame, a "snapshot" sequence is initiated by the Base Frame. Strobe \$SNO strobes $ICTC_{0-17}$ into $ICTA'_{0-17}$. The conditions determining whether $ICTA'_{17}$ is a "0 or "1" are the same as the normal case. When \$SN1, the second snapshot strobe is received, $ICTA'_{0-17}$ is transferred to $ICTA_{0+17}$ subject to the same conditions as shown for normal tracking of $ICTA_{17}$. However,

COMPANY CONFIDENTIAL
GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh. 9-87 Sh. No. 9-86

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.5.2 - contd

if the fault detected was an operations unit fault (divide check, overflow, parity error in operand), or parity on a nonoperations unit instruction operand, the original ICTA₀₋₁₇ is not changed. This means that when the expected SCU instruction in the processor fault vector is encountered, ICTC₀₋₁₇ is stored for nonoperations unit faults except parity, or ICTA₀₋₁₇ for operations unit faults and nonoperations unit parity faults.

9.3.5.3 RCU Instruction Tracking

When an RCU instruction is encountered, the Control Frame is restored to its status prior to the condition which caused some fault. All the status flags (PA, PI, PZ, etc.) are restored from the ICTA'₀₋₁₇ counter.

The "repeat" flags (FT, FD, FL, RF) are restored directly from the ZDI data input lines at the same time that the ICTB counter is loaded via the ICT switch. When the sixth word designated by the RCU instruction is brought into the I-register, bits 36-71, a normal two-instruction fetch takes place in the Control Frame moving ICTB₀₋₁₇ to ICTC₀₋₁₇ and the I-register to the Y- and C-registers.

9.3.6 CT-REGISTER (See 43D163387 sheet 29)

The CT-register is a six bit register used to hold the tag field (bits 30-35) of the instruction or indirect word for IR and IT address modification, and the delta field for "repeat" instructions. For R-type address modification, the CT-register contains the tag field of the instruction word, but this field is not used.

Data for the CT-register comes from the ZI bus for normal address preparation and from the ICTA' register during restore operations resulting from an RCU instruction. Use of the the tag field is as specified for the particular address modification employed.

Whenever the "repeat" instructions are encountered, the delta field is strobed into the CT-register at the

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-88 Sh. No. 9-87

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.6 - contd

end of the PA cycle of the "repeat" instruction. When the repeated instruction(s) is being executed, only R and RI modification is permitted and the tag is not strobed into the CT-register because it will destroy the delta field required for the "repeat" operation. At the time of termination for the repeated instruction(s), the delta field is forced to look like an R modifier. This is done by resetting CT₀ (bit 30 of the tag field of an instruction or indirect word) and preventing the possibility of an erroneous IR tag which could cause further action. Refer to the logic diagram for the exact terms which control the strobe and data.

9.3.7 RE-RO-REGISTERS; \$ORY, \$ZOR AND B CONTROL (See 43D163387 sheet 27)

Each time the Control Frame sends an operation code to the Operations Unit, it must send a strobe \$ORY indicating that the operation code is ready at the input to the O-register in the Operations Unit. The Operations Unit replies with a strobe \$YRY when the instruction has been decoded, and the operand is presented to the Operations Unit. The Control Frame then knows that another instruction may be sent; provided certain other conditions are met. The dispatching of an even or odd operation code, to the Operations Unit, is controlled by the "B" flip-flop in the Control Frame; if "B" is reset, an even instruction is sent, if set, an odd instruction is sent.

Because four instructions can be contained in the Control Frame, the possibility exists (and will generally be the rule rather than the exception), that the Control Frame is one or two instructions ahead of the Operations Unit and has an instruction ready before the Operations Unit can accept it. Therefore, the Control Frame is provided with two registers (RE and RO) to buffer the even and odd operation codes. These registers hold the nine-bit operation code that is to be put on the ZOR bus to the Register Frame of the Operations Unit. Which register is selected (RE or RO) depends on the state of the "B" flip-flop. As soon as the Operation Unit can accept an operation code, it sends back strobe \$YRY to the

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-89 Sh. No. 9-88

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.7 - contd

Control Frame allowing the "B" flip-flop to switch the other operation code on the ZOR bus. The "normal" sequence is to load both the RE and RO buffers and send the even operation code to the Operations Unit. When the Operations Unit sends back \$YRY, the Control Frame sends the odd operation code. The RE and RO buffers are then reloaded from the next instruction pair in the Y- and C-registers. The Operations Unit is allowed to get no more than three instructions behind the Control Frame under any conditions because of inhibits on the CU/OU interface term equation for \$C. The only deviation from the "normal" sequence, is when there is a nonoperations unit instruction in the even instruction location. In this case, the RE and RO buffers will not get loaded with the even instruction, but a flag is set to indicate that the even instruction was a nonoperations unit instruction. When the prepare cycle for the odd instruction is in progress, and provided it is an operation unit instruction, then the RO buffer will be loaded at the same time that the "B" flip-flop switches the RO buffer output to the ZOR bus.

If the nonoperations unit instruction was in the RO (odd) buffer, then the "B" flip-flop is not toggled switching RO to the ZOR bus.

Concurrent with the switching of the RE or RO buffer outputs to the Operations Unit, \$ORY is also generated by the Control Frame to indicate that an operation code is on the ZOR lines. Strobe \$ORY is generated from the same strobe that generates \$ZOR BUFFER, but is delayed 108 nanoseconds after \$ZOR BUFFER, to enable the data on the ZOR bus lines to settle. A \$ZOR Δ is also generated to strobe the ICTA' register approximately 90 nanoseconds after \$ZOR.

9.3.7.1 Status Flag

Whether or not the RE and RO buffers will be strobed with a new operation code, and when the B flip-flop is toggled, is defined by the state of five status flags:

- 1) ONR -- Operations Unit Not Ready

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-90 Sh. No. 9-89

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.7.1 - contd

- 2) EOC -- Even Operation Code
- 3) OOC -- Odd Operation Code
- 4) EOF -- Even Operation Code First
- 5) NOS -- Not Operations Unit Sequence

These status flags are explained in reference to their set and reset equations as follows:

- 1) ONR set = \$POC
reset = \$YRY+XF+WF+TRMF

Strobe \$POC is a strobe that precedes \$ORY and is the result of satisfying all conditions to issue \$ORY to the Operations Unit. When the ONR flag is set, the B flip-flop state cannot be changed, and additional \$ZOR and \$ORY strobes cannot be generated. This condition will remain until the Operations Unit is not busy; indicated by a \$YRY which resets the ONR flag. Strobe \$YRY is only received when the Operations Unit is able to accept a new operation code.

- 2) $\overline{\text{EOC}}$ set = $\$Z \cdot (\text{EA} \cdot \overline{\text{IC}})$
reset = $\$ORY \cdot \overline{\text{B}} + \text{WF}$

The terms $\text{EA} \cdot \overline{\text{IC}}$ indicate that an effective address for an operand, for the instruction in the Y-register, is available from the BS-adder. Strobe \$Z is defined as follows:

$$\$Z = \$PRR \cdot [\overline{\text{TRMF}} \cdot \overline{\text{Y}} \cdot \overline{\text{ROS}} \cdot (\text{T} + \text{PN}(\text{RET} + \text{RTD}))] + \$\Delta\text{AM2} [\overline{\text{TRMF}} \cdot \text{TSX}_n + \text{ROS} + \text{Y} \cdot \overline{\text{T}}]$$

The terms associated with \$PRR represent the conditions for slow operations unit instructions and allow \$Z to be generated approximately 340 nanoseconds later than for fast operations unit instructions. Inhibit terms are for: not terminating a "repeat" instruction ($\overline{\text{TRMF}}$); not a direct operations unit operand ($\overline{\text{Y}}$); not operations unit stores or read-alter-rewrite type instructions ($\overline{\text{ROS}}$). The RET and RTD instructions are executed in part within

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-91 Sh. No. 9-90

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.7.1 - contd

the Control Unit while the T term defines nonoperations unit instructions

All terms associated with $\$ \Delta AM2$ are for conditions which represent fast operations unit instructions and consequently require less time for decodes to settle and operations to be executed. Transfer and set index register (TSX_n) is a special case transfer that is treated as a fast operations unit instruction.

Resetting of the EOC flag depends on $\$ORY$ and $\bar{B}$; indicating that whenever the Operation Unit is sent a strobe indicating that an operation code from the Y-register is on the ZOR bus, that EOC will be reset.

- 3) $EOC \text{ set} = \$Z (EA \cdot IC)$
 $\text{reset} = \$ORY \cdot B + WF$

The conditions for the set and reset of the EOC flag is identical to the EOC flag except for the term IC and B.

When IC is true, the operation code is from the C-register. When B is true, the odd operation code has been sent.

- 4) $EOF \text{ set} = EOC \cdot \overline{EOC}$
 $\text{reset} = \$ORY \cdot \bar{B} + WF$

This means that EOF is set when an even operation code from the Y-register is to be sent to the Operations Unit, before the odd operation code. The only time that EOF will not be set is if the even operation code was not an operations unit instruction, and EOC did not get set.

- 5) $NOS \text{ set} = \$R \cdot [PI \cdot XDE + (EA + \overline{TRGO} \cdot CT)$
 $(T + PN(RT + RTD))]$
 $\text{reset} = \$ORY + WF$

The group of terms for the set equation for the NOS flag shows that NOS is set for all nonoperations unit instructions; or portions of the execution of some instructions that involve the Operations Unit and Control Unit.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-92 Sh. No. 9-91

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.7.2 B Flip-Flop Control, \$ZOR Buffer and \$ORY Generation

The signal levels that control the state of the B flip-flop also generate a pre-strobe called \$POC. Strobe \$POC eventually generates \$ZOR and \$ORY, although not necessarily both at the same time. Resetting the B flip-flop and thereby sending the even operation code to the Operations Unit is accomplished when all the terms for an even OU instruction are true; specifically:

$$\begin{aligned} B \text{ reset} &= \$POC \cdot [(\overline{ONR} \cdot \overline{EOC} \cdot \overline{EOF}) & (1) \\ &\quad \cdot \overline{TRMF} \cdot \overline{EIF} \cdot \overline{IC} \cdot (Y + TSX + ROS) \cdot \overline{TMCH} = 1] & (2) \end{aligned}$$

- 1) This equation represents the general case for resetting the B flip-flop and sending the even operation code for an operation unit instruction to the Operations Unit.
- 2) These terms represent a special case where a terminate for a "repeat" type instruction, occurs after the process to send the operation code for a fast operations unit type instruction to the Operations Unit, has already started. For this condition, it is too late to stop the generation of \$POC and the B flip-flop from being reset and sending the even operation code; so B is inhibited from being reset. The B flip-flop is not changed because the Operations Unit cannot accept an operation code until housekeeping and cleanup functions for the "repeat" instruction takes place within the Operations Unit.

When all the terms for resetting the B flip-flop are present and \$POC is generated, \$ZOR is generated to strobe the even and odd operation code into the RE and RO buffers. Strobe \$ORY is also generated by \$POC, but occurs approximately 144 nanoseconds after \$ZOR.

$$\$ZOR = \$POC (EVEN + NOS \cdot ODD) \quad (3)$$

- 3) Indicating that \$ZOR is generated for an even operations unit instruction odd operations unit instruction that was preceded by a nonoperations unit instruction. When \$ZOR is generated, both the even and odd operation code is strobed into the RE and RO buffer.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-93 Sh. No. 9-92

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.7.2 - contd

Whenever \$ZOR is generated, it is delayed 54 or 90 nanoseconds and used to strobe ICTA' with the address of the instruction waiting in the RE-buffer (even instructions) or RO-buffer (odd instruction when preceded by a nonoperation unit instruction).

The conditions which set the B flip-flop are:

$$B \text{ set} = \$POC \left[\frac{(\overline{ONR} \cdot OOC \cdot \overline{EOF})}{\cdot \overline{TRMF} \cdot EIF \cdot IC \cdot (Y + TSX + ROS) \cdot TMCH = 1} \right] \quad (4)$$

- 4) This equation represents the general case for setting the B flip-flop, when the odd operation code is going to be sent to the Operations Unit.
- 5) The groups of terms in this equation are identical to equation (2) with the exception of IC which represents the odd rather than the even instruction.

As before, when a \$POC is generated \$ORY is also generated: but \$ZOR will not necessarily be generated.

The conditions which set the B flip-flop are:

$$B = \overline{ONR} \cdot OOC \cdot \overline{EOF}$$

In this case, the B flip-flop is set, \$POC is generated, but no \$ZOR unless the even operation code had been a nonoperation unit (NOS true) instruction. However, \$ORY is generated approximately 100 nanoseconds after \$POC.

Control of the RE and RO switches to the ZOR bus is a function of the B flip-flop. However, the B flip-flop outputs may be inhibited by the RCU and RTD instructions.

$$\phi \text{ RE/ZOR} = \overline{B} \cdot ((RCU + RTD) \cdot GBO)$$

$$\phi \text{ RO/ZOR} = B \cdot ((RCU + RTD) \cdot GBO)$$

When $(RCU + RTD) \cdot GBO$ is true, the controls $\phi \text{ RE/ZOR}$ and $\phi \text{ RO/ZOF}$, are inhibited and a return instruction (630_g) is forced on the ZOR bus, so the Operations Unit can load its registers and indicators.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-94 Sh. No. 9-93

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.7.3 Timing Diagram

Figure 9.3.7.3 is a timing diagram for the sequences that take place in loading the RE- and RO-buffers, and is representative of the normal case, that is, both RE and RO-buffers, and is representative of the normal case, that is, both RE and RO loaded at the same time.

9.3.8 MFREE COUNTER AND MRD CONTROL (See 43D163387 sheet 11)

As mentioned previously, the Control Frame has the capability of being one, two or three instructions ahead of the Operations Unit. In addition, all operands sent to the Operations Unit are buffered in the M-register of the Operations Unit until they are moved into the working registers. However, during multiply operations, the M-registers is used as a working register. This means that the Control Frame must continually check the status of the M-register before attempting to send an operand to the Operations Unit. The Control Frame is provided with a MFREE counter to keep track of the number of operands sent to, or on the way to, the M-register of the Operations Unit. This register keeps track of up to three operands; one in the M-register of the Operations Unit, one in the Direct Buffer in the Base Frame, and one on the way from memory. The third operand will only be requested from memory if the Operations Unit is doing a "short" instruction and will be free when the operand arrives.

9.3.8.1 Count-Up Cycle

The count-up cycle input for each MFREE counter stage is basically the same for each stage as can be seen from the logic diagram.

Each stage is set as successive operations unit operands are requested from memory. Counting of the operands is as shown on the logic diagram and in Table 9.3.8.1

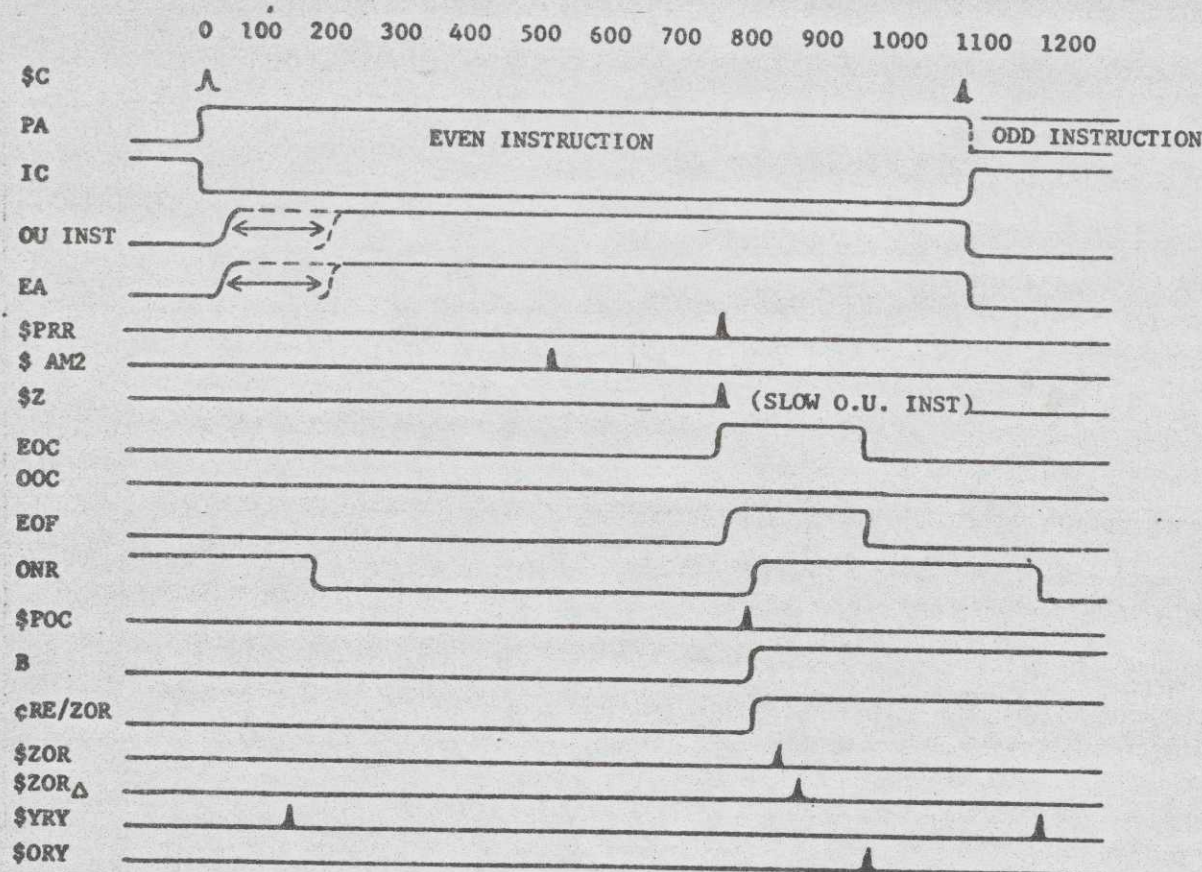
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Spec. No. M50EB00107

Cont. on Sh. 9-95 Sh. No 9-94

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR



NOTE:

- 1) It is assumed that the Y- and C-registers are loaded with slow Operations Unit instructions and the Y-register operand address will be prepared first.

FIG. 9.3.7.3 RE, R0 Buffer Loading, Timing Diagram

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-96 Sh. No. 9-95

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 9.3.8.1 MFREE Counter States

Count	MFREE ₂	MFREE ₁	MFREE ₀
0	0	0	0
1	0	0	1
2	0	1	1
3	1	1	1

9.3.8.2 Count-Down Cycle

The count-down cycle is somewhat different than the count-up cycle due to the asynchronous nature of the Control Frame and the Operations Unit, and the possibility of trying to count down and up at the same time. Two flip-flops, MRD1 and MRD2, are used to generate a \$FREE which resets or counts down each stage of the MFREE counter, when the M-register signals that it is free. Counting down begins with stage MFREE₂ and will end with stage MFREE₀, if no new operands are fetched for the Operations Unit before the M-register is free.

The MRD1 flip-flop sets with strobe \$(AF) \cdot (FNR)\$. Strobe \$(AF)\$ is general strobe generated within the Operations Unit; FNR indicates that the Operations Unit cannot accept a direct operand. Generally, FNR is true. When MRD1 sets, it will set MRD2 and generate \$FREE to count down the MFREE counter, provided the term $\overline{SRF_2} \cdot \overline{SRF_3}$ is true. This term indicates that a \$R has been issued for an operand and MFREE has been counted up. If $\overline{SRF_2} \cdot \overline{SRF_3}$ is true, the MRD2 stage will not be set until $\overline{SRF_2} \cdot \overline{SRF_3}$, to allow MFREE to be counted up before being counted down, thus preventing a race condition. Strobe \$FREE resets MRD1 which resets MRD2, and all circuits are ready to respond to the next \$(AF) \cdot (FNR)\$ combination indicating the M-register is free.

9.3.8.3 Timing Diagram

Figure 9.3.8.3 is a timing diagram of the MFREE count-up and count-down cycles.

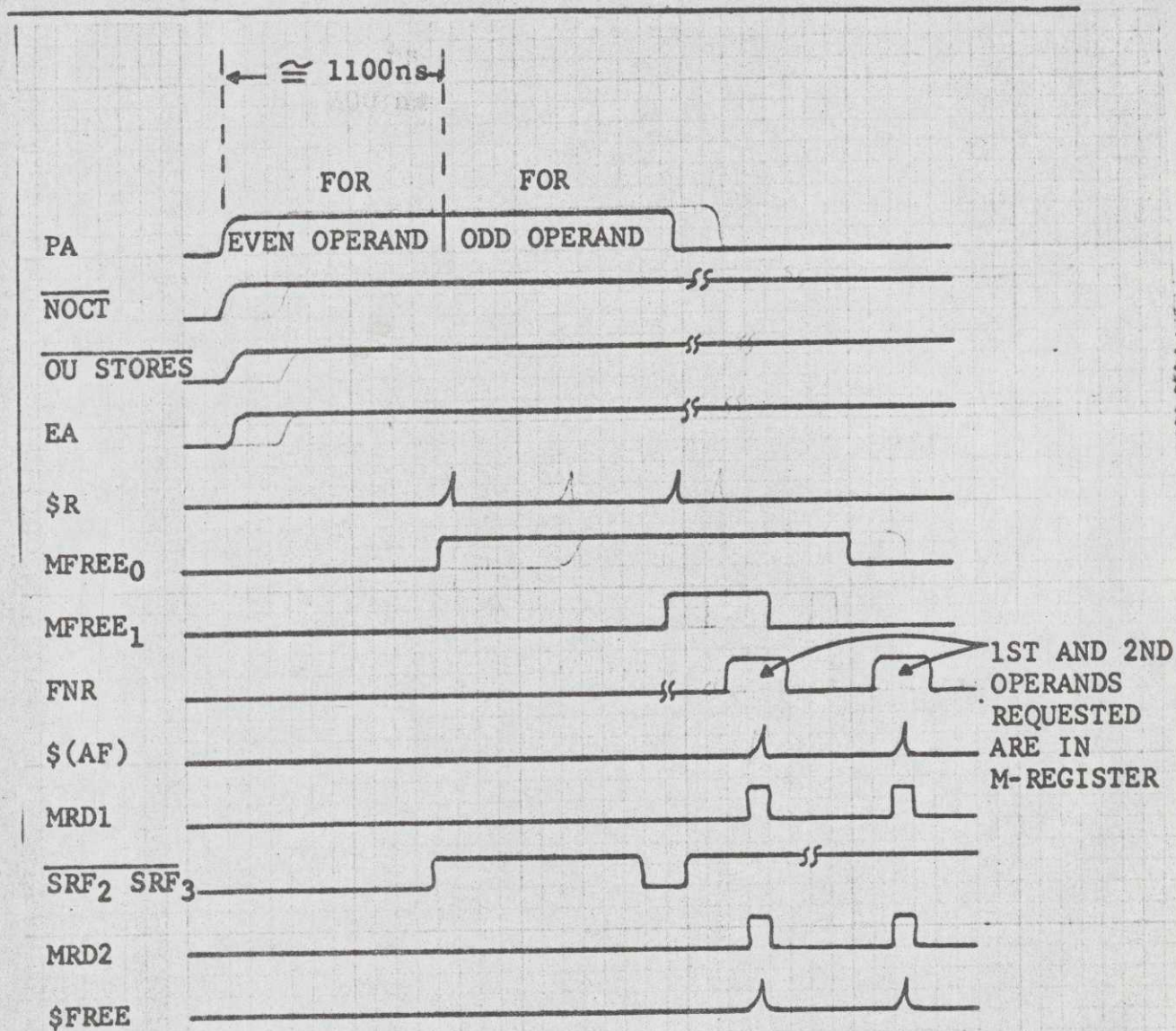
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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-97 Sh. No. 9-96

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR



NOTES:

1. Two operands are requested from memory before the first operand is used by the Operations Unit.
2. Counter shows count of two, then is decremented.
3. Relationships are not to scale.

FIG. 9.3.8.3 MFREE Counter, Timing Diagram

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.9-98 Sh. No.9-97

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.9 TMCH COUNTER (See 43D163387, sheets 43, 44)

The Control Frame contains a three-stage counter to keep track of the number of operands currently in, or on the way to the Operations Unit as distinguished from the MFREE counter which keeps track of the operands sent to the M-register. This counter is designated TMCH, and is counted up every time an operand is sent to the Operations Unit, as signified by receipt of \$R (and certain other conditions) generated for an interrupt. Counting down of TMCH is done by a \$DOWN which is a function of conditions which indicate that the Operations Unit has finished or will not complete an operation.

9.3.9.1 Count-Up Cycle

The three stages of the TMCH counter are set by the following equations:

set conditions

$$TMCH_0 = (EA \cdot \overline{TMCH_1} \cdot \overline{NOCT}) \cdot \$R$$

$$TMCH_1 = (EA \cdot TMCH_0 \cdot \overline{NOCT}) \cdot \$R$$

$$TMCH_2 = [(EA \cdot TMCH_1 \cdot \overline{NOCT}) + (EA \cdot TMCH = 1 \cdot NOP)] \cdot \$R$$

This shows that the TMCH counter will be counted up one stage at a time with each interrupt for an operations unit operand. There is a special case where TMCH will indicate a count of 1+NOP (No Operation Performed). Table 9.3.9.1 shows the count in the different stages for all conditions.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-99 Sh. No. 9-98

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 9.3.9.1 TMCH Counter States

Count	TMCH ₂	TMCH ₁	TMCH ₀
0	0	0	0
1	0	0	1
2	0	1	1
3	1	1	1
1+NOP	1	0	1

The TMCH counter will only be allowed to go to three, in the case of short operations unit instructions.

9.3.9.2 Count-Down Cycle

The count-down cycle is quite different from the count-up cycle because of the asynchronous nature of the Operations Unit and the Control Frame, and the possibility of strobing TMCH up and down at the same time. Each stage is counted down (reset) beginning with TMCH₂, or when a "repeat" instruction is terminated as indicated by level DR.

reset conditions

$$\text{TMCH}_2 = \$\text{DOWN} + \text{DR}$$

$$\text{TMCH}_1 = \$\text{DOWN} \cdot \overline{\text{TMCH}_2 \Delta} + \text{DR}$$

$$\text{TMCH}_0 = \$\text{DOWN} \cdot \overline{\text{TMCH}_1 \Delta} + \text{DR}$$

Strobe \$DOWN and the conditions which generate is are defined as follows:

$$\$DOWN = \Delta C \cdot (\text{TRMF} \cdot \overline{\text{WN}}) \quad (1)$$

$$\Delta C = \$PDN \quad (2)$$

$$\$PDN = \text{LST}_2 \cdot (\text{SEP} \cdot \overline{\text{DVCK}} \cdot \text{FOLF} \cdot \text{LST}_1 \Delta) \quad (3)$$

$$\text{LST}_2 = \overline{\text{SRF}_2} \cdot \text{SRF}_3 \cdot \overline{\text{SFF}} \cdot \text{LST}_1 \quad (4)$$

$$\text{LST}_1 = (\$LAST + \$FOLF + \$DVCK) \cdot \overline{\text{WF}} \quad (5)$$

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Spec. No. M50EB00107

Cont. on Sh. 9-100 Sh. No. 9-99

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

9.3.9.2 - contd

Analyzing the equations from number (5) and working toward the generation of \$DOWN:

- 5) \$LAST, \$FOLF and \$DVCK indicate that the Operations Unit is finished with an operand, or there is a overflow or divide check for an arithmetic operation which also terminates operations unit action. Any one of these strobes unconditionally sets LST_1 , unless a fault is about to be processed.
- 4) LST_2 is set whenever SRF_2 and SRF_3 do not occur together and no fault has been detected. This effectively inhibits any action to generate \$DOWN beyond this point.

SRF_2 set = $(EA \cdot \bar{T}) \cdot \PRR

reset = $\$R_{\Delta}$

SRF_3 set = $\$IF + \$SSRF$

reset = $\$R_{\Delta} + \$RSRF$

These equations show that LST_2 will be set whenever \$R is not about to be issued for an interrupt. This \$R would count up the TMCH counter, at possibly the same time that it was being counted down. That is, SRF_2 "sets" on the interface term coming true for a operations unit operand, SRF_3 is set on \$IF and reset by \$RSRF if the Interface Frame must perform an appending operation. Strobe \$SSRF from the Interface Frame then sets SRF_3 again, inhibiting the setting of LST_2 and stopping \$DOWN. Resetting of both SRF_2 and SRF_3 will occur at $\$R_{\Delta}$ time; approximately 100 nanoseconds after the \$R for the current interrupt has counted up the TMCH counter. IF LST_1 is set when SRF_2 and SRF_3 are reset, LST_2 is set. Summarizing: LST_2 is set only if there is no chance of \$R for the interrupt, and \$DOWN resulting from a \$LAST, strobing the TMCH counter at the same time.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-101 Sh. No. 9-100

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.9.2 - contd

- 3) Strobe \$PDN (pre-down) is generated as a result of LST_2 , LST_1 and not having any of the other conditions:
 - SEP -- Instruction with parity error was not completed.
 - DVCK -- Divide check on arithmetic operation of last operations unit instruction.
 - FOLF -- Overflow on the arithmetic operation last executed by Operation Unit.
- 2) The level ΔC , initiated by \$PDN and terminated by ΔC delayed through additional delay inverters to its own reset input, is to allow enough time for portions of the Z-function logic to be reset before TMCH is strobed down.
- 1) Finally, if there is a $TRMF \cdot \overline{WN}$ condition, no \$DOWN is generated, unless $TRMF \cdot \overline{WN}$ comes true before ΔC resets. When the terminate condition is serviced for a "repeat" type instruction, then a level called DR is generated which resets the TMCH counter to a zero state.

9.3.10 STORE COMPARE (EX) FUNCTION (See 43D163387 sheet 37)

The store-compare function (EX-function) indicates that the current instruction being processed will store data into one of the memory locations from which the remaining instructions contained in the Control Frame are located. If such is the case, the instructions following the one currently being prepared by the Control Frame must be refetched. Whether one, or two instructions must be refetched depends on the results of the comparison between the current instruction being prepared, and the remaining instructions. The comparison is made by comparing the operand address of the instruction in the Y-register to the memory location of the instructions in the C-register (EX_1 level) and the I-register (EX_2 and EX_3 levels). Similarly, when preparing the instruction in the C-register, the operand address is compared

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Spec. No. M50EB00107

Cont. on Sh.9-102 Sh. No.9-101

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.10 - contd

to the memory location of the instructions in the I-register (generation of EX₂ and EX₃ levels only).

The comparisons are made in the following manner and will cause the following events to occur:

- EX₁ level:
- 1) ICTC₀₋₁₆ compares with BS₀₋₁₆.
 - 2) BS₁₇ = "1" indicating the address is for the C-register or a STAQ instruction is decoded which effects the C-register.
 - 3) The PBR contents equals the TBR contents indicating that the addresses of the instructions compared are in the same segment.
 - 4) The Control Frame is preparing a store or read-alter-rewrite type instruction.
 - 5) The Y-register did not contain an execute double instruction. This is to prevent a store-compare level when an XED instruction is "brute forced" into the Y- and C-registers because of a fault.

When the conditions in 1 through 5 above are satisfied, the EX₁ level is generated and causes:

- 6) An XEC instruction with an R modification (designating the ICTC register contents to repull the instruction for the C-register) to be "brute forced" into the C-register.
- 7) Inhibits the strobing of the Y-register for the refetched instruction coming into C-register via the V-switch, ZDI bus, and VTB switch.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.9-103 Sh. No.9-102

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

9.3.10 - contd

EX₂, EX₃ levels.

- 8) ICTB₀₋₁₆ compares with BS₀₋₁₆.
- 9) The PBR contents equals the TBR contents indicating that the addresses of the instructions compared are in the same segment.
- 10) The Control Frame is preparing a store or read-alter-rewrite instruction.

When the conditions in 8 through 10 are satisfied and the EX₂, EX₃ levels are generated, the following occurs:

- 11) The EXI flip-flop is set to remember that a comparison was made on the I-register.
- 12) If the comparison was made when preparing the instruction in the Y-register, the instruction in the C-register is executed first, then the I-register is repulled using the ICTB address that is sent to the BS-adder. As the instructions are brought in they are routed around the I-register to the Y- and C-registers. When EX₂ and EX₃ is generated, the ICTB address is not updated in the normal manner (adding +1 to both the YS- and BS-adders) until the EX₂ and EX₃ levels are removed and the EXI flip-flop is reset. The EXI flip-flop was used to generate EX₂ and EX₃. In cases where the instruction in the C-register is being compared against the I-register, and EX₂ and EX₃ levels are generated, no waiting is necessary and the I-register instructions are repulled as previously described.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.9-104 Sh. No.9-103

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.10 - contd

In those cases where the I-register is normally re-fetched (transfers, PI cycles or faults) the EXI flip-flop is reset, since the ICTB address is either different or invalid.

9.3.11 Z FUNCTION (See 43D160212 sheet 5, and 43D163387 sheets 19,20)

The purpose of the Z-function is to hold up any address modification for an instruction being prepared by the Control Unit, when the Operations Unit is changing a register that is required for the address modification. Only R, and RI type address modification in the instruction word and IR modification in the indirect word is considered, since only these modifiers can designate a register that may be required by the Operations Unit to execute an instruction; specifically, the X0-X7, A- and Q-registers. Generation of the Z-function is accomplished by comparing the tag field of the instruction or indirect word currently being prepared, that is on the DW⁰⁰₀₈ 1B (ZI) bus, with the coded operation code of the previous one or two instructions that had been sent to the Operations Unit. These instructions are saved in the Z1 and Z2 registers (see the Z-function circuitry on the upper righthand corner of 43D160212 sheet 5). The specific code of the tag field on the ZT bus and coded operation code field that is saved in the Z1 and Z2 registers is shown in Table 9.3.11. Note in Table 9.3.11, that the RI and IR address modification types IC, DU, DL and N are omitted since these modifications do not use the X-, A- or Q-register.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-105 Sh. No. 9-104

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 9.3.11 Comparison of Codes on ZT Bus
with Codes in Z1, Z2 Registers

Tag Reg. Designates	Tag				Code in Z1, Z2 (Note 1)				Reg. Designated by Code in Z1
	ZT ₀	ZT ₁	ZT ₂	ZT ₃	ZI ₀	ZI ₁	ZI ₂	ZI ₃	
X0	1	0	0	0	1	0	0	0	X0
X1	1	0	0	1	1	0	0	1	X1
X2	1	0	1	0	1	0	1	0	X2
X3	1	0	1	1	1	0	1	1	X3
X4	1	1	0	0	1	1	0	0	X4
X5	1	1	0	1	1	1	0	1	X5
X6	1	1	1	0	1	1	1	0	X6
X7	1	1	1	1	1	1	1	1	X7
AU	0	0	0	1	0	0	0	1	A
AL	0	1	0	1	0	0	1	1	AQ
QU	0	0	1	0	0	0	1	0	Q
QL	0	1	1	0	0	0	1	1	AQ

NOTE:

- 1) Coding of Z1 is identical to Z2.
- 2) Register designators for ICTC, DU, DL and N are ignored.

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Spec. No. M50EB00107

Cont. on Sh. 9-106 Sh. No. 9-105

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

5

9.3.11 - contd

Generation of the Z-function (if one is to be generated) is done in the following manner: (See 43D160212 sheet 5, and 43D163387 sheets 19,20)

- 1) An instruction is being prepared and the resultant address preparation cycle causes the operation code to be placed on the ZI bus (ZI_{0-8}).
- 2) When the preparation cycle is completed and a \$R is generated, the ZI-register is strobed with the appropriate bits of the ZI bus that may designate one of the X0-7 or A- or Q-registers. The bit positions being selected are the same for all instructions and represent all cases where the X0-7, A- and Q-registers are designed by the operation code.
- 3) Address preparation is now started for the next instruction. At this time the tag portion of the ZI bus is switched to the Z comparator via the ZI_{14-17} (ZI/ZT) switch.
- 4) If ZI compares with the ZT bus then a BZFN1F (Z-function) level is generated. If no comparison no level.
- 5) The Z-function level in conjunction with \$^AAM1, sets a DZ flip-flop in the \$R, \$C generation circuits which inhibits the generation of \$IF, and the resultant strobes to start the Interface Frame. When the Interface Frame is not started no \$IFF is received in the Control Frame to set the IFR flip-flop in the \$R, \$C generation circuits and any further strobes are inhibited. (See paragraph 9.3.1 for this discussion in detail.)
- 6) No further address preparation takes place until the Operations Unit sends a \$LAST. This strobe causes the TMCH counter circuits to generate a \$DOWN that eventually resets the DZ flip-flop and caused strobe \$IF to be generated, starting the strobe chain again. Resetting the ZI register takes place as a function of level ΔC (generated in the process of producing a \$DOWN) and the TMCH counter equal 1, or 1 + NOP state.

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Spec. No. M50EB00107

Cont. on Sh.9-107 Sh. No.9-106

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.3.11 - contd

The foregoing steps (1 through 6) presuppose that the Operations Unit was not busy and that there was a comparison on the Z1-register. If there was no comparison on the Z1-register, the following takes place:

- 7) The Z1-register is moved into the Z2-register concurrent with strobe \$PRC (a strobe that precedes \$R).
- 8) The Z1-register is strobed by \$R and then will contain the decoded operation code field of the instruction that is currently being processed and present on the ZI bus.
- 9) When address preparation is started for the third instruction (two instructions sent to the Operations Unit, and two codes in the Z1, Z2-registers) the tag field of this instruction is compared to the Z1- and Z2-registers and possible generation of the Z-function.
- 10) When the Operations Unit produces a \$LAST resulting in a \$DOWN, the Z2-register is reset, since the Operations Unit is finished with the instruction that is represented by the code in the Z2-register.
- 11) The sequence of steps continue until the Operations Unit is caught up to the Control Frame (as far as instructions that effect the X0-7, A- and Q-registers) or the tag fields of new instructions do not specify the X0-7, A- and Q-registers.

For instructions that involve RI or IR address modification, the new tag(s) brought in by the indirect word(s) are compared with the Z1- and Z2-registers, but the operation codes in the Z1- and Z2-registers are not changed until a new instruction is being processed. There is a special case when the Z-function is generated for "repeat" type instructions. Whenever one of the repeated instructions designates any index register, the Z-function is generated until the Operations Unit is finished with the current instruction execution.

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Spec. No. M50EB00107

Cont. on Sh. 9-108 Sh. No. 9-107

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

9.3.11 - contd

When an index register is specified by the operation code and tag field of one of the repeated instructions, both the index register designated by the instruction and the index register designated by tag field of the instruction must be changed. To do this, the Operations Unit executes the index instruction; then the delta portion of the "repeat" instruction is added to the index register used for address modification of the repeated instruction(s) (see the RPT, RPD and RPL instruction descriptions for address modification of the repeated instructions.) This means that for "repeat" type instructions with address modification, the Control Unit never gets ahead of the Operations Unit.

9.3.12 MAINTENANCE/CONTROL PANEL FUNCTIONS

A re-examination of the Maintenance/Control Panel covered in Section 3.0 of Part I of this EPS shows that there is a considerable array of indicators, switches and pushbuttons. Only those switches that are directly involved with the Control Frame circuits will be discussed. The indicator lamps for the various registers and status flags are not involved with any circuit actions within the Control Frame, since the voltages used to control the indicator lamps are tapped from the circuits involved without effecting any operation. The only circuit actions that take place, allow different registers to be displayed on the same set of indicator lamps. This is done by manual switching from the Maintenance/Control Panel proper (see 43D139956). The following switches and pushbuttons on the Maintenance/Control Panel effect the Control Frame operation: REPEAT EXECUTE; STOP; OU/CU OVERLAP OFF; CF TEST CLOCK; EXECUTE SWITCHES; EXECUTE (pushbutton); STEP (pushbutton); TEST ENABLE; and STEP ENABLE rotary switch positions: OFF, PROG, CU and MEM.

9.3.12.1 Switch Functions (Refer to 43D163387 sheets 39,40,41 for details)

TEST ENABLE - when this switch is activated the switch functions on the Maintenance/Control Panel are enabled.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 9-109 Sh. No. 9-108

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

9.3.12.1 - contd

This enable level is used in various places throughout the Control Frame circuitry as can be noted from the logic diagrams.

CF TEST CLOCK - When this switch is activated, the generation of strobes in the \$C, \$R generating circuits is speeded up by approximately 18 nanoseconds for marginal timing checks.

OU/CU OVERLAP OFF - When this switch is activated, the Control Frame will not proceed in advance of the Operations Unit. This is accomplished by inhibiting the interface term for strobe generation until the TMCH counter equals zero.

STOP - This is a momentary ON switch. When depressed, the STOP flip-flop is set. When STOP is set, a fault sequence is initiated by the processor fault logic in the Base Frame, the normal "snapshot" sequence in preparation for fault servicing takes place, and the Processor stops in a WF cycle. When the STOP switch is released a DIS instruction (616₈) is forced onto the ZDI bus via the normal input data switch (V switch). The STOP flip-flop is reset by \$C·WF and the DIS instruction is "brute forced" into the Y- and C-registers. A PA cycle is entered for the DIS instruction, then terminated by the next \$C produced from the \$C, \$R logic. The result is the Processor initialized and waiting for an interrupt.

EXECUTE (pushbutton) - Depressing the EXECUTE pushbutton initializes the Processor by setting a pre-stop (PST) flip-flop that forces the STOP flip-flop to set thereby causing the same actions as depressing the STOP switch. When PST resets itself, approximately 180 nanoseconds later, a DIS instruction is forced on the ZDI bus and the Processor is initialized. Releasing the EXECUTE pushbutton causes the EXF flip-flop to be set, causing the processor fault logic to initiate an execute fault. The normal "snapshot" and fault sequence is entered, resulting in a "brute-forced" XED instruction with a fault address corresponding to the execute fault-vector pair in memory, forced into

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.9-110 Sh. No.9-109

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

9.3.12.1 - contd

the Y- and C-registers. Any action once the fault-vector pair is pulled from memory depends on the instructions contained in the fault-vector.

EXECUTE SWITCHES - When the EXECUTE SWITCHES switch is activated, the contents of the INSTRUCTION switches on the Maintenance/Control Panel are forced into the Y- and C-registers instead of the instructions contained in the fault-vector pair in memory corresponding to the execute fault.

REPEAT EXECUTE - The REPEAT EXECUTE switch works in conjunction with an oscilloscope gate input at the processor SYNC PANEL located on the physical cabinet frame behind the Maintenance Panel. Application of an oscilloscope gate as a trigger source, and with the REPEAT EXECUTE, and EXECUTE SWITCHES, switches activated, causes the Processor to be initialized, do an execute fault from the INSTRUCTION switches and keep repeating the sequence.

STEP pushbutton - Depressing the STEP pushbutton sets the SPR flip-flop. When SPR is set it allows \$PRII which generates \$R (providing all other strobe generation conditions are met) and starts the Processor. SPR is normally set when the Processor is running and is only reset with \$PRR and the conditions generated by the STEP ENABLE switch.

STEP ENABLE switch:

PROG position - strobe \$PRII's are stopped since SPR is reset in the first PA cycle entered by the Processor preventing any more \$R's from being generated by the \$R, \$C generation circuits.

CU and MEM positions - this position stops \$R's in the same manner and the PROG position except that SPR is reset during any prepare cycle except PR.

The net effect is that for the PROG position, the Processor can step from \$C·EA to \$C·EA; in CU position from \$C to \$C; and in MEM position from \$INT to \$INT.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
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PHOENIX, ARIZONA

Spec. No. M50EB00108

Cont. on Sh. 10-1 Sh. No. 9-110

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

9.4 BASIC OPERATING SEQUENCES

To be supplied later

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Spec. No. M50EB00107

Cont. on Sh. 10-2 Sh. No. 10-1

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.0 APPENDING UNIT DETAILED OPERATION

The Appending Unit contains the hardware registers and control logic to handle all functions concerned with the selection of address pointers to segments and pages of segments in memory, and the actual communication between the Processor and Memory. To perform the necessary functions requires two frames of logic: the Interface Frame and the Base Frame. The Interface Frame is concerned with the final address preparation for data to and from memory, and the Base Frame is concerned with storing the address pointers in one of its various registers and supplying this information when requested by the Control Unit.

Additional functions performed by each frame is explained under the applicable description of the particular frame. One note of information, however; the majority of the Processor fault logic is contained in the Base Frame due to space limitations in the Control Unit. Pertinent information is discussed following the Base Frame Detailed Operation.

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Spec. No. M50EB00107

Cont. on Sh. 10-3 Sh. No. 10-2

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1 INTERFACE FRAME DETAILED OPERATION

The Interface Frame, as its name implies, is the link or interface between the Processor and the Memory Controller(s). The processor must be capable of communicating with from one to eight Memory Controllers with various size core memories. It must be able to select the proper Memory Controller and to respond to signals from any of the Memory Controllers.

The Interface Frame consists of address preparation logic, data out logic, and memory selection and response logic. It handles all communication with the Memory Controllers except receipt of data on the Data In bus, which is handled by the Base Frame. It performs the final address preparation in one of three modes, and makes all fault checks having to do with that address. It develops all control signals for, and sends them to, the proper Memory Controller. It responds to all control signals from the Memory Controller.

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Spec. No. M50EB00107
Cont. on Sh. 10-4 Sh. No. 10-3

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.1 FUNCTION

The Interface Frame consists of three major groups: Address Preparation, Data Output, and Memory Control.

The address preparation logic is constructed around two registers, an adder, and a comparator. The Descriptor Register (DES₀₋₃₅) receives all address appending words from core memory (for example, PTW). The format of this register is the same as for the word that it holds. This register and its associated logic receives a SDW, PTW, etc. from the core memory via the ZDI lines in the Base Frame. The data is held for use by the adder and is sent, for storage, to the Associative Memory. The Descriptor Generator generates the descriptor field for PTWs and checks for all faults except Out of Bounds. The Address Register (ADR₀₋₂₃) receives all address of words to be retrieved for core memory. This address is used by the memory selection logic and is sent to all Memory Controller ports. The RS-adder (RS₀₋₁₇) is used in the preparation of addresses. It accepts addresses or portions of addresses from the DES Register, the Base Frame, the Control Frame, the Associative Memory, and the Maintenance Panel, and adds or concatenates the pieces to form the final address, which is stored in the ADR Register. The Boundary Comparator (BC₀₋₁₁) checks the address against the boundary field except in Absolute mode, where it checks the address against the upper limit of physical core memory. This logic is able to operate in any one of three modes as determined by the start pulse received from the Control Frame.

Absolute Mode (\$\$AB)--In this mode the address from the Control Frame is the final address and it is merely passed through the RS-adder and stored in ADR₀₋₂₃. The address is checked by BC₀₋₁₁ to see if it is within the physical limits of memory. If it is not, an OOB faults occurs.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-5 Sh. No. 10-4

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.1 - contd

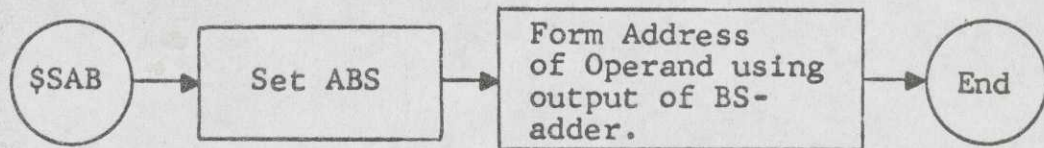


Fig. 10.1.1 Absolute Mode Addressing,
Flow Chart

Append Without Associative Memory (\$SAP)--In this mode the address from the Control Frame must go through the appending process. During the appending the Associative Memory does not operate and all information is retrieved from core memory. All appending words are checked for faults and the final appending word is checked for access violation. The final address is checked against the boundary field to see if it is within the specified boundary. If it is not, an OOB fault occurs. See Fig. 10.1.1a.

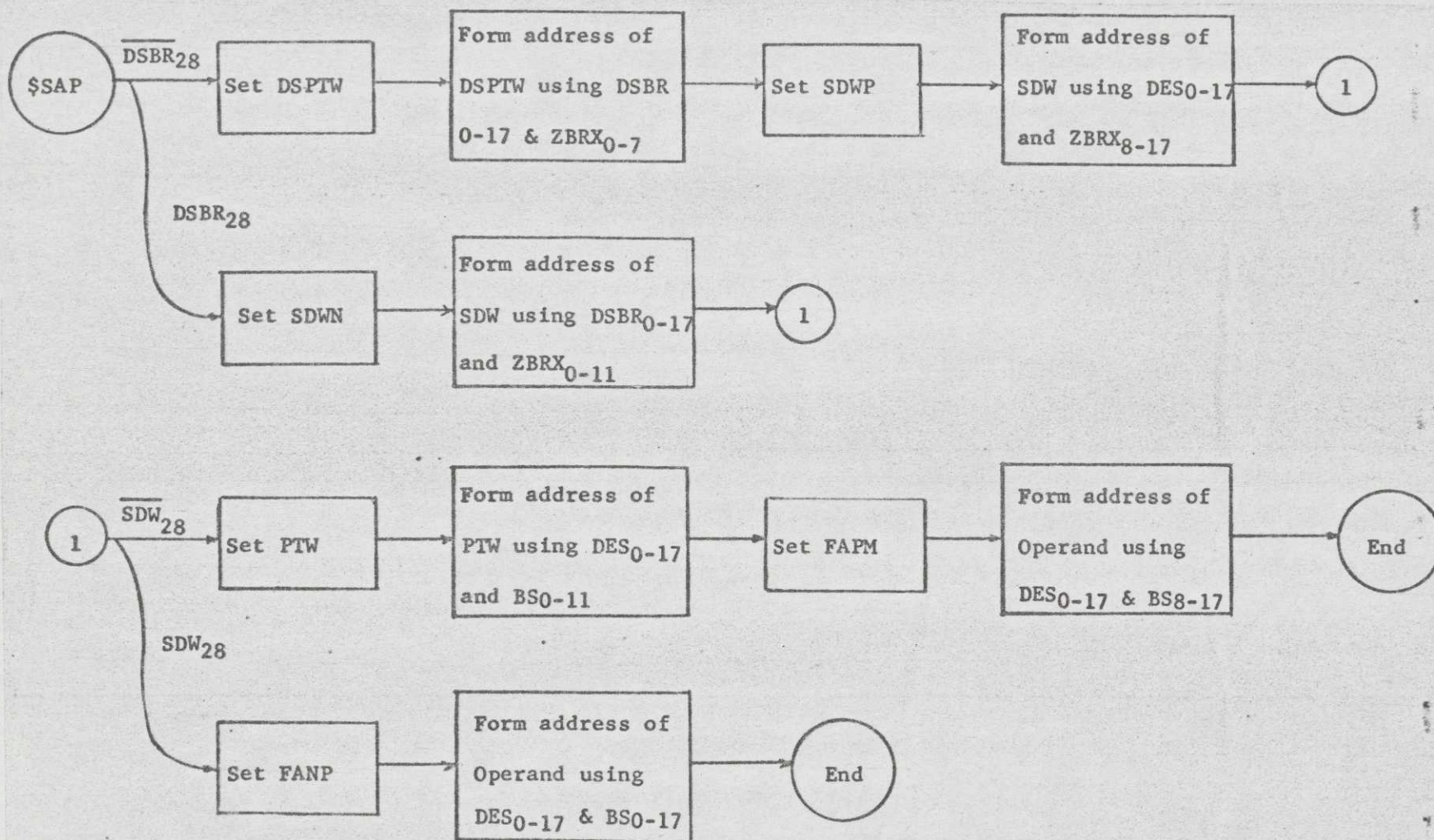


Fig. 10.1.1a Append Without Associative Memory
 Flow Chart

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-7 Sh. No. 10-6

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.1 - contd

Append with Associative Memory (\$AAM)--In this mode the address from the Control Frame must go through the appending process. The Associative Memory will be searched, and if the required information (PTW or SDW) is located it will be used in the address preparation. If the information is not there it must be retrieved from core memory. Only the appending words retrieved from core memory are checked for faults. All final appending words are checked for access violations. See Fig. 10.1.1b.

There is also a special case dealing with the written bit. Whenever a page is altered by a store or RAR operation the written bit of its PTW must be set to a "1." If the PTW was retrieved from core memory, this presents no problem but if it was obtained from the Associative Memory, a special sequence must be gone through. Even though the PTW is in the Associative Memory, a special sequence must be gone through. Even though the PTW is in the Associative Memory its address in core memory must be developed in order to set its written bit.

The final address is checked against the boundary field to see if it is within the specified boundary. If it is not, an OOB fault occurs.

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

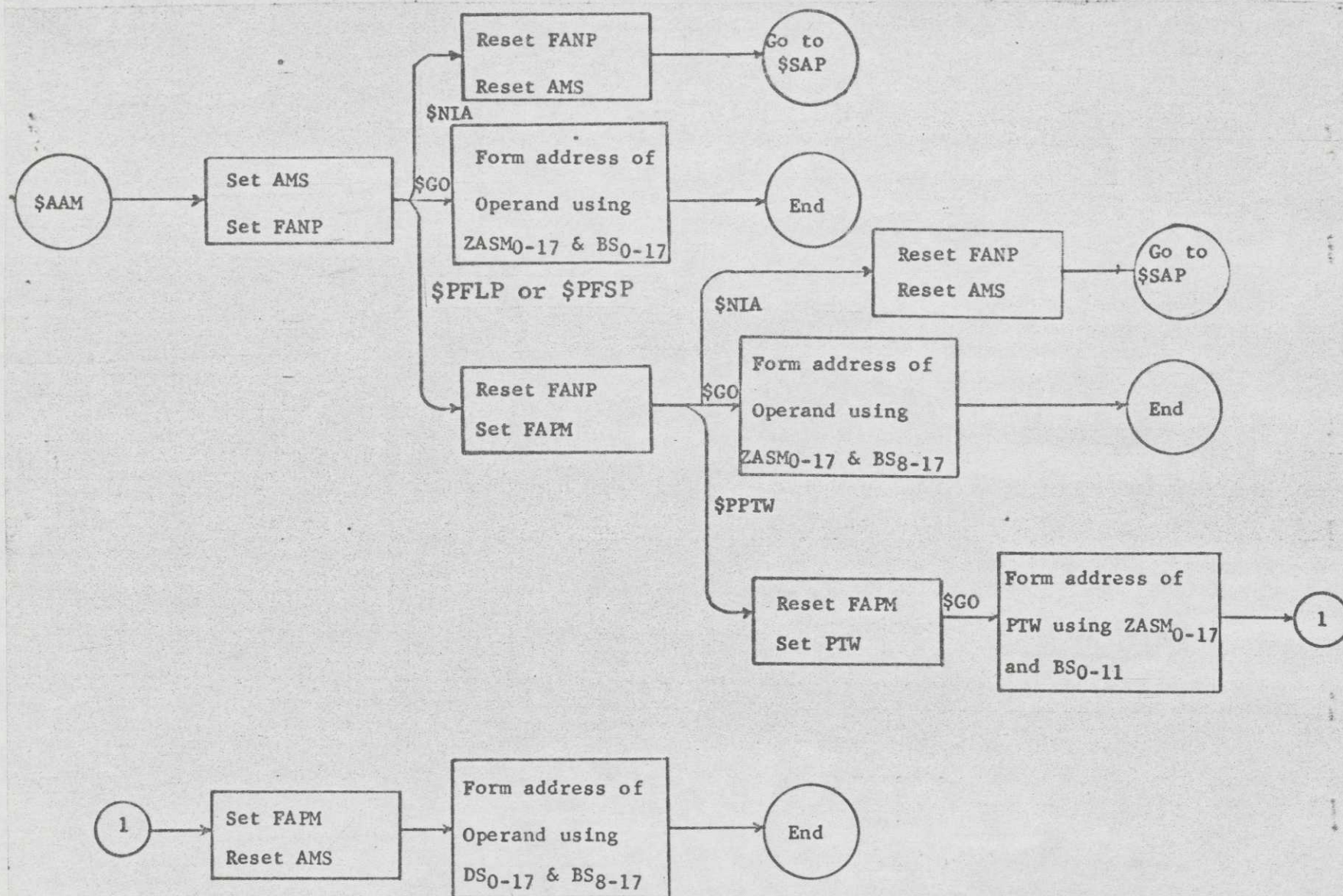


Fig. 10.1.1b

Append With Associative Memory,
 Flow Chart

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Spec. No. M50EB00107

Cont. on Sh. 10-9 Sh. No.10-8

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.1 - contd

The data out logic is constructed around a 72-bit register (DOR₀₋₇₁). The input to this register comes from the ZD₀ lines of the Base, Control, and Register Frames, from the Read Out switch of the Associative Memory, and from the RS Adder. Any information that is to be stored in core memory will be placed in this register (except written bits). It is also used during the "snapshot" portion of a fault to retain certain information until it can be stored by a SCU instruction. The output of this register goes to a switch that selects either the upper half (DOR₀₋₃₅) or the lower half (DOR₃₆₋₇₁) and presents it to all memory ports.

The memory control logic is constructed around various control flip-flops, registers, and strobe generators. The DIR₁ and DIR₂ flip-flops are used to determine which one of the eight memory ports will be used. The registers are:

- 1) Command (CMD₀₋₃) -- The specific action to be taken by the Memory Controller is determined by this register.
- 2) Zone (ZONE₀₋₇) -- The particular portion of a word to be altered is determined by this register.
- 3) Illegal Action (IAL₀₋₂) -- If an illegal action has occurred in the Memory Controller this register will be set with a code indicating what occurred.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-10 Sh. No.10-9

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.1 - contd

This portion of the logic must accept an operation code from the Control Frame and an address from its own address preparation logic, determine what is needed with the core memory (for example, appending word, read or store operand, instruction) and set up its Command Register to tell the Memory Controller what to do. It must also determine if a 6- or 9-bit character operation is in progress, and if so, set up the Zone Register accordingly. The IF must issue requests and other control strobes, and must recognize illegal actions and store the corresponding code.

10.1.2 INTERFACE

The Interface Frame has external interface with the Memory Controller(s) and internal interface with the other five frames.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-11 Sh. No.10-10

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.2.1 External

The Interface Frame has identical connections to eight ports. It is connected to two of the three 50 pin connectors, which make up a port. Each port may or may not be connected to a Memory Controller. Open connections will have no affect on the associated logic. The following lines are used to send information to the Memory Controller(s).

- 1) Data Lines (36) -- These lines are used to transfer data from the Data Out Register.
- 2) Address Lines (24) -- The address that is prepared by the Interface Frame and stored in the Address Register is placed on these lines to specify the location in core storage that is to be involved in a read/write operation.
- 3) Zone Lines (8) -- These lines are used to select the 6- or 9-bit characters to be involved in any Clear-Write command or the rewrite portion of a Read-Alter-Rewrite command. A "1" on a Zone Line indicates that the corresponding character is to be altered. A "0" on a Zone Line indicates that the corresponding character is to remain unchanged. Table 10.1.2.1a correlates the Zone Line with the character and bit positions it controls.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-12 Sh. No. 10-11

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.2.1 - contd

Table 10.1.2.1a Zone Lines vs. Character
and Bit Positions

Zone Line	Character	Bit Positions
0	0	0 - 5
1	1U	6 - 8
2	1L	9 - 11
3	2	12 - 17
4	3	18 - 23
5	4U	24 - 26
6	4L	27 - 29
7	5	30 - 35

- 4) Interrupt Line -- The Interface Frame selects the Memory Controller to be utilized and then sends out a pulse on this line to that Memory Controller. This pulse, called strobe interrupt, requests access to the memory.
- 5) Double Precision/Rewrite Line -- Double Precision Store and Read-Alter-Rewrite operations require two memory cycles. When the Interface Frame determines that the second 36-bit word of a Double Precision Store or the altered word of a RAR is on the data lines it places a pulse on this line signifying that the memory can start its second cycle.

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Spec. No. M50EB00107

Cont. on Sh. 10-13 Sh. No. 10-12

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.2.1 - contd

- 6) Protect Line -- Certain operations involving memory can only be done if the Processor is executing a Master Procedure (including Absolute mode). The Interface Frame places a "1" on this line when the Control Frame is in Master mode.
- 7) Command Lines -- The Interface Frame receives the operation code from the Control Frame, determines the type of memory operation required and places that command code on these lines. There are ten possible commands as shown in Table 10.1.2.1b.

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GENERAL ELECTRIC COMPANY
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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-14 Sh. No. 10-13

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.2.1 - contd

Table 10.1.2.1b Memory Commands

Mnemonic	Command	Code			
		A	B	C	D
RRS,SP	Read-Restore, Single Precision	0	0	0	0
RRS,DP	Read-Restore, Double Precision	0	0	0	1
CWR,SP	Clear-Write, Single Precision	0	1	0	0
CWR,DP	Clear-Write, Double Precision	0	1	0	1
RAR	Read-Alter-Rewrite	1	0	0	0
RMSK	Read Execute and Channel Interrupt Mask Registers	0	0	1	0
SMSK	Set Execute and Channel Interrupt Mask Registers	0	1	1	0
SXC	Set Execute Interrupt Cells	1	1	1	0
CON	Connect	1	1	0	0
XEC	Execute	1	1	0	1

The following lines are used to receive information
from a Memory Controller:

- 1) Cycle Started Delayed Line -- A pulse (strobe PIN) on this line indicates that the Memory has granted access to the Processor, and that

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-15 Sh. No.10-14

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.2.1- contd

it has received the control information on the Command, Address, and Zone Lines. The Interface Frame need not retain the information on these lines past this pulse. On Double Precision or Read-Alter-Rewrite operations two pulses will be received by the Processor. The second pulse indicates that the control information for the second part of the operation has been received.

- 2) Data Available/Stored Line -- A pulse on this line has different meanings depending upon the operation being performed. During any read operation or the first half of a Read-Alter-Rewrite operation a pulse on this line indicates that the Memory has placed the required data on the Data Lines to the Processor and that it will remain there for 200 nanoseconds. During any store operation or the second half of a Read-Alter-Rewrite operation a pulse on this line indicates that the required data on the Data Lines to Memory has been received and that the Processor can now change these lines. During any Double Precision operation two pulses will be received one for each half of the double precision word.
- 3) Strobe Connect Line -- A pulse on this line indicates that the Memory Controller has received a connect command to this port from the Control Processor.
- 4) Illegal Action Strobe Line -- A pulse on this line indicates that the Memory has correctly completed its operation or that an illegal action has taken place. The code on the Illegal Action Lines tells which is which (see next paragraph). This pulse is used to sample the Illegal Action Lines.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-16 Sh. No.10-15

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.2.1 - contd

- 5) Illegal Action Lines (3) -- These lines indicate the specific reason that a Illegal Action Strobe was issued. The code on these lines is valid only at the time that this strobe occurs. The codes and their meanings are:

<u>A B C</u>		<u>Priority</u>
1 0 0	Not Control Processor	1
0 1 0	Not Master Mode	2
0 1 1	Parity Error	3
0 0 0	No Illegal Action	4

- 6) Execute Interrupt Line -- An unmasked Interrupt Cell in the Memory Controller will place a "1" on this line. It will set the corresponding flip-flop of the IPR-Register in the Control Frame.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-17 Sh. No.10-16

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.2.2 Internal

The internal interface will be considered one frame at a time and are listed in Tables 10.1.2.2 and 10.1.2.2a.

Table 10.1.2.2 Interface Frame Inputs

<u>Mnemonic</u>	<u>Description</u>
Register Frame	
DDOOD-DD35D (ZDORF0-35)	DATA OUTPUT BUS
QDPPD(\$DP)	STROBE DOUBLE PRECISION
Arithmetic Frame	
FIO9C (PAR MASK)	INDICATES PAR. ERR FAULT TRAP DISABLED
FIO7C (TALLY RUNOUT)	LAST TALLY WAS ZERO
Associative Memory	
DC30E-DC35E(ZADS30-35)	ASSOC. REG. DESCRIPTOR BUS
BA55E(ZAU55)	ASSOC.REG.ADJUST USAGE BIT BUS
BE54E(ZEF54)	ASSOC.REG.EMPTY/FULL BIT BUS
BU56E-BU59E(ZSUC56-59)	SELCTD.USAGE COUNTER BUS
DA00E-DA17E(ZASM0-17)	ADDRESS MOD.64 BUS
DB18E(ZBB18)	BASE BIT BUS
DB19E-DB26E(ZABD19-26)	BOUNDARY BUS
DC27E-DC29E(ZADS27-29)	ASSOC.REG. DESCRIPTOR BUS
DT36E-DT53E(ZPTR50-53)	ASSOC.POINTER BUS
QNIAE(\$NIA)	NO INFORMATION AVAILABLE PULSE
QSSFE(\$SF)	START FETCH PULSE
QSULE(\$SET FA PMLP)	SET UP FAPM (LP) FETCH PULSE
QSUPE(\$SET PTW)	SET UP PTW FETCH PULSE
QSUSE(\$SET FA PMSP)	SET UP FAPM (SP) FETCH PULSE
QWBCE(\$START WBC)	START WRITTEN BIT CYCLE

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 PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-18Sh. No.10-17

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

Table 10.1.2.2 Interface Frame Inputs - contd

<u>Mnemonic</u>	<u>Description</u>
Control Frame	
BEADB(EA)	PREPARED ADDRESS IS FOR OPERAND
BFLSB(RPTS)	REPEAT FLAG DECODE FD OR FT
BIPCB(PC)	PREPARE INTERRUPT
BISIB	INHIBIT STROBE INTERRUPT
BMPAB(FPA)	FAULT OR EXECUTE INT. IN PA CYCLE
BSFTB	INHIBIT STROBE IF
BSPAB(CSET PA)	LEVEL TO SET PA
BSPIB(CSET PI)	LEVEL TO SET PI
BSPNB(CSET PN)	LEVEL TO SET PN
BSPRB(CSET PR)	LEVEL TO SET PR
BSPTB(CSET PT)	LEVEL TO SET PT
BSWNB(CSET WN)	LEVEL TO SET WN
BTBCB	WF AND STOP
BTRGB(TRG01)	TRANSFER GROUP SUB 1 DECODE
BYCFB	DIRECT TYPE OPERATION
DD00B-DD35B(ZDOCF0-35)	CONTROL FRAME DATA OUTPUT BUS
DW00B-DW17B(ZIO-17)	INST.REG.DECODE BUS
ECICB	CONNECT
ECTO B-ECT5B(CT0-5)	TAG BIT STORAGE REGISTER
EMLSB	MULTIPLE LOAD STORE
EMSYB(MSY)	MASTER/SLAVE FLAG
EPROB-EPR7B(IPRO-7)	INTERRUPT PRIORITY REGISTER
EXSFB(XSF)	EXECUTE SWITCHES FAULT
MBOOB-MB17B(BS0-17)	ADDRESS BASE ADDER
QAAMB(\$AAM)	START ASSOCIATIVE APPENDING STROBE
QCFFB(\$CFF)	COMPARE STROBE
QESRB	EA AND STROBE R
QPRCB(\$PRC)	PRE STROBE C
QSABB(\$SAB)	START ABSOLUTE STROBE
QSAPB(\$SAP)	START APPENDING STROBE
QSCAB(\$SCA)	STROBE TO SCANNER LOGIC
QZCCB(\$C)	GENERAL STROBE
QZDPB(\$DP)	DOUBLE PRECISION STROBE

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-19 Sh. No.10-18

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 10.1.2.2 Interface Frame Inputs - contd

Mnemonic

Description

Base Frame

BAB4F	PH.4 SIG. TO PORTS A&B INTERLACE
BABIF	PH.2 OR 4 SIG. TO PORTS A&B INTERLAC
BCD4F	PH.4 SIG. TO PORTS C&D INTERLACE
BCDIF	PH.2 OR 4 SIG TO PORTS C&D INTERLACE
BEF4F	PH.4 SIG. TO PORTS E&F INTERLACE
BEFIF	PH.2 OR 4 SIG. TO PORTS E&F INTERLAC
BGH4F	PH.4 SIG. TO PORTS G&H INTERLACE
BGHIF	PH.2 OR 4 SIG. TO PORTS G&H INTERLAC
BNPFF	PARITY ERROR
BP04F(<u>GP4</u>)	RECOGNIZE BUFFER FILLING PI PARITY FAULT
BPETF(PRB=TBR)	CONTENTS OF PBR EQUALS CONTENTS OF TBR
BPIEF	PARITY (SPECIAL)
BPSIF	INHIBIT STROBE PARITY
BRPAF-BRPHF(<u>PORT ON</u>)	A-H PORT ON
BSFFF(<u>SFF</u>)	STOP FOR FAULTS
DD00F-DD35F(<u>ZDOBF0-35</u>)	36-BIT BASE FRAME DATA OUT BUS
DI00F-DI35F(<u>ZDIO-35</u>)	DATA INPUT BUS
DX00F-DX17F(<u>ZBRX0-17</u>)	BASE REGISTER EXTERNAL BUS
EGBOF(GB0)	GENERAL BASE INSTRUCTION F/F
EN03F-EN05F(<u>INC3-5</u>)	INCREMENTOR REGISTER
ERSTF	RESET
ESNOF(SN0)	SNAPSHOT ZERO F/F
ESN1F(SN1)	SNAPSHOT ONE F/F
EWFOF(WF)	WAIT FOR FAULT
FS00F-FS28F(<u>DSBR0-28</u>)	29-BIT DESCRIPTOR SEG.BASE REGISTER
QBRYF(\$BRY)	BASE READY PULSE
QDPBF(\$DP)	DOUBLE PRECISION STROBE
ZSNOF(\$SN0)	SNAPSHOT ZERO PULSE
QSNZF(\$SN1)	SNAPSHOT ONE PULSE

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GENERAL ELECTRIC COMPANY
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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-20 Sh. No. 10-19

COMPANY CONFIDENTIAL

TITLE: ENGINEERING PRODUCT SPECIFICATION No. M50EB00107
GE-645 PROTOTYPE PROCESSOR
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Cont. on Sh. 10-20 Sh. No. 10-19

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 10.1.2.2 Interface Frame Inputs - contd

<u>Mnemonic</u>	<u>Description</u>
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Maintenance Panel

Table 10.1.2.2 Interface Frame Inputs - contd

SA00T-SA05T	ABSOLUTE ADDRESS SWITCH
SAMST	ASSOCIATE MEMORY OFF
SIHFT	INHIBIT FAULT SWITCH
SSCUT	STEP CU SWITCH
SMMT	STEP MEMORY SWITCH
SSPGT-SA05T	STEP PROGRAM SWITCH
SSTPT	STEP SWITCH
STSTT	TEST SWITCH
SSCUT	STEP MEMORY SWITCH
SMMT	STEP PROGRAM SWITCH
SSPGT	STEP SWITCH
SSTPT	TEST SWITCH
STSTT	

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-21 Sh. No. 10-20

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 10.1.2a Interface Frame Outputs

<u>Mnemonic</u>		<u>Description</u>
Arithmetic Frame		
EHTAM(HTAL)		CHANGE TALLY RUNOUT IND
QDSTM(\$DS)		DATA STORED PULSE
QZPRM(\$PARITY)		PARITY PULSE
Associative Memory Frame		
BMSTM		DECODE FOR STORE OR RAR CYCLES TO ASSOC. MEM.
BPTLM(WPTWL)		WRITE PTW LARGE
BPTSM(WPTWS)		WRITE PTW SMALL
BSDWM(WSDW)		WRITE SDW
EWBSM		SET WRITTEN AND USED BIT
FDOOM-FD35M(DES0-35)		36-BIT DESCRIPTOR REGISTER
QDAMM(\$DAAM)		DATA AVAILABLE PULSE
QRELM(\$RELEASE)		RELEASE PULSE
Base Frame		
BFAAM	FA	FINAL ADDRESS FETCH(FAPM+FANP+ABS)
EIFAM-EIFCM	IARA-C	3-BIT ILLEGAL ACTION REG.
EP20M-EP27M	DIR20-7	PORT SELECTION F/F
EPINM		PREPARE INTERRUPT
ESPFM	STE	STEP
ESSIM		STOP STROBE INTERRUPT
FD30M-FD32M		DES REGISTER
QAVFM	\$AVF	ACCESS VIOLATION FAULT PULSE
QBORM	\$BORY	START BASE OPERATION PULSE
QDFCM	\$DF	DIRECTED FAULT PULSE
QDSTM	\$DS	DATA STORED PULSE
QIASM	\$SIAL	SPECIAL ILLEGAL ACTION PULSE
QICFM	\$ICF	ILLEGAL CLASS FAULT PULSE
QINTM	\$INT	STROBE INTERRUPT
QOBFM	\$OBF	OUT OF BOUNDS FAULT PULSE
QOCNM	\$CON	CONNECT PULSE FROM ALL PORTS
QOIAM	\$IAL	ILLEGAL ACTION PULSE FROM ALL PORTS
QPINM	\$PIN	STROBE PIN
QRSFM	\$RSF	IF READY TO FAULT PULSE
QSDAM	\$DA	DATA AVAILABLE PULSE

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-22 Sh. No. 10-21

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 10.1.2.2a Interface Frame Outputs - contd

<u>Mnemonic</u>	<u>Description</u>
Control Frame	
BDPCM	DOUBLE PRECISION COMMAND
BFAAM($\overline{\text{FA}}$)	FINAL ADDRESS FETCH(FAPM+FANP+ABS)
BLSRM	END MULTIPLE INST.
BIAOM-BIA3M($\overline{\text{IBA0-3}}$)	INTERRUPT BLOCK ADDRESS BITS 0-3
BRMLM(CRESET MLSF)	RESET MLSF F/F
DAIPM-DHIPM($\overline{\text{IPO-7}}$)	EXTERNAL INTERRUPT PRESENT-PORTS A-H
EMS2M(MSF2)	NEXT INST.PR.MASTER/SLAVE MODE BUFFE
ERDYM($\overline{\text{SRDY}}$)	PROC.READY FOR STEP FLAG
FNOOM-FN17M(SCA0-17)	SCANNER BITS 0-17
MA15M-MA17M(RS15-17)	RS-ADDER BITS 15-17
QDSTM($\overline{\text{\$DS}}$)	DATA STORED PULSE
QIAZM($\overline{\text{\$IAZ}}$)	STROBE ILLEGAL ACTION
QIFFM($\overline{\text{\$IFF}}$)	INTERFACE FRAME FINISHED PULSE
QINTM($\overline{\text{\$INT}}$)	STROBE INTERRUPT
QOPNM($\overline{\text{\$PIN}}$)	STROBE PIN
QPRIM($\overline{\text{\$PRI}}$)	STROBE C
QSDAM($\overline{\text{\$DA}}$)	STROBE DATA AVAILABLE
QSRFM($\overline{\text{\$RSRF}}$)	APPNDG.FETCH STARTED PULSE
QSSFm($\overline{\text{\$SSRF}}$)	FINAL FETCH STARTED PULSE
Maintenance Panel	
EABSM(ABS)	ABSOLUTE MEMORY FETCH CYCLE
EAMSM(AMS)	ASSOC.MEMORY SEQUENCE FLAG
EAPEM	APPEND PARITY ERROR
EBFRM(BFR)	BASE FRAME READY F/F
EBIFM(BIF)	BASE INSTRUCTION SPECIAL CONTROL F/F
ECFRM(CFR)	CONTROL FRAME READY F/F
EDAFM(DAF)	DATA AVAILABLE/STORED FLAG
EDDFM(DDAF)	DOUBLE PRECISION FLAG
EDINM(DPIN)	DOUBLE PRECISION PIN FLAG
EDPBM	DESCRIPTOR PAGE TABLE WORD
EDPTM(DSPTW)	DESC.SEG.PG.TBL.WD.MEMORY FETCH CYCL
EFANM(FANP)	FINAL ADDRESS(NON-PAGED MEMORY FETCH CYCLE
EFAPM(FAPM)	FINAL ADDRESS(PAGED)MEMORY FETCH CYCLE
EPTBM	PAGE TABLE WORD
ESDBM	SEGMENT DESCRIPTOR WORD

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-23 Sh. No. 10-22

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 10.2.2a Interface Frame Outputs - contd

Mnemonic

Description

Maintenance Panel

EHTAM(HTAL)	TALLY RESULT HOLDING F/F (ZERO/ NON-ZERO)
EIFRM(IFR)	INTERFACE FRAME READY F/F
ELPFM(LPF)	PAGE SIZE FLAG
EMLSM(MLSF)	MULTIPLE LOAD/STORE INST.FLAG
EMS2M(MSF2)	NEXT INST.PR.MASTER/SLAVE MODE BUFFER
EMSFM(MSF1)	NEXT INST.PR.MASTER/SLAVE MODE F/F
EPINM(PIN)	MEMORY READY F/F
EPTWM(PTW)	PG.TBL.WD.MEMORY FETCH CYCLE
ESDNM(SDWN)	SEG.DESC.WD.FETCH-NONPAGED DESC.SEGMENT
ESDPM(SDWP)	SEG.DESC.WD.FETCH-PAGED DESC.SEGMENT
ESWUM(SWU)	SET WRITTEN/USED BIT CYCLE
EWAWM(WAW)	WAIT FOR APPENDING WORD FLAG
EWBFM(WBF)	SET WRITTEN/BIT FLAG(IF DETECTED)
EWBSM(WBS)	SET WRITTEN BIT SEQUENCE FLAG (IF DETECTED)

Relay Box

EA00M-EA23M(ADRO-23)	24-BIT ADDRESS REGISTER
EIFAM-EIFCM(IARO-2)	3-BIT ILLEGAL ACTION REGISTER
EP10M-EP17M(DIR1 0-7)	PORT SELECTION
EP20M-EP27M(DIR2 0-7)	PORT SELECTION
EZ00M(ZONE0)	ZONE REGISTER BIT 0
EZ02M(ZONE2)	ZONE REGISTER BIT 2
EZ03M(ZONE3)	ZONE REGISTER BIT 3
EZ05M(ZONE5)	ZONE REGISTER BIT 5
EZL1M(ZONE L1)	ZONE REGISTER BIT L1
EZL4M(ZONE L4)	ZONE REGISTER BIT L4
EZU1M(ZONE U1)	ZONE REGISTER BIT U1
ECMAM-ECMDM	COMMAND REG.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-24 Sh. No. 10-23

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

Table 10.1.2.2a Interface Frame Outputs-contd

Mnemonic

Description

Relay Box

EZU4M(ZONE U4)	ZONE REGISTER BIT U4
FD00M-FD35M(DESO-35)	36-BIT DESCRIPTOR REGISTER
F000M-F071M(DORO-71)	72-BIT DATA OUTPUT REGISTER
MA00M-MA17M(RSO-17)	SUM OUTPUTS OF RS ADDER

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-25 Sh. No. 10-24

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.3 ADDRESS PREPARATION

The Interface Frame's function in address preparation is to take the address formed by the Control Frame and convert it to the address required by the Memory Controller. This can be done in several ways depending upon the mode of operation. In general, the Interface Frame takes the address from the Control Frame and using information obtained from the Base Frame, Associative Memory, and Core Memory as required, forms the final address that is presented to the Memory Controller. This discussion will deal strictly with the portion of the Interface Frame operation from the initiation of an address preparation cycle to the issuance of a \$INT for an operand or instruction pair. This does not include any address modification that takes place in the Control Frame, or any of the other functions of the Interface Frame. The three modes of operation, each started by a pulse from the Control Frame, are:

- 1) Absolute - started by \$SAB.
- 2) Append Without Associative Memory - started by \$SAP.
- 3) Append With Associative Memory - started by \$AAM.

See charts and timing diagrams at end of this section.

10.1.3.1 Absolute Mode

The absolute mode of operation is characterized by the Interface Frame accepting the address presented by the Control Frame as the final address. If it is for an operand or instruction it is also considered a final effective address.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-26 Sh. No. 10-25

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.3.1 - contd

After the Control Frame has embarked on a prepare address cycle, it will send a \$SAB to the Interface Frame. This pulse will set the ABS flip-flop and enter a delay line to emerge as \$IFR.. During the time interval between ABS set and \$IFR the following events occur:

- 1) FA becomes true.
- 2) (EA) (FA) becomes true if this is a final effective address for an operand.
- 3) $\phi BS_{0-11}/RS_{6-17}$, $\phi BS_{12-17}/ADR_{18-23}$, $\phi RS_{0-17}/ADR_{0-17}$ all come true switching the output of the BS-adder with six leading zeros to the input to the Address Register (ADR_{0-23}).
- 4) \$IFF will be sent to the Control Frame to set its IFR flip-flop.

\$IFR will set the Interface Frame Ready flip-flop in the Interface Frame. When the Base Frame and the Control Frame become ready, (in this case it will happen at the same time), the BFR and CFR flip-flops will set. At this time a last pulse detector will generate a \$A, which will:

- 1) Be delayed and then generate a \$ALS.
- 2) Generate a \$INT.
- 3) Reset BFR and CFR.
- 4) Generate \$ADR.

\$ALS will reset IFR, and ABS.

\$ADR will strobe the address into the Address Register.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-27 Sh. No.10-26

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.3.1- contd

\$INT is sent to the selected Memory Controller and it will:

- 1) Generate \$DOR if required.
- 2) Reset PIN.

This completes the absolute mode.

10.1.3.2 Append Without Associative Memory

This mode of operation is characterized by the Interface Frame taking the address presented by the Control Frame and appending it to a nonpaged SDW or to a PTW to form the final address. All intermediate steps deal with information from core memory and registers in the Base Frame. This mode is only used if a store Associative Memory operation is in progress or if the TEST ENABLE and ASSOC MEM OFF switches on the Maintenance Panel are enabled. There are many possible combinations of ways to arrive at a final address. The shortest and longest will be discussed.

Assume that the Segment Descriptor Table is not paged and that an instruction pair is to be fetched from a nonpaged segment. After the Control Frame has embarked on a prepare address cycle it will send a \$SAP to the Interface Frame. (DSBR₂₇ and DSBR₂₈ both = 1, SDW₂₇ and SDW₂₈ both = 1).

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-28 Sh. No.10-27

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.3.2 - contd

\$SAP will generate a \$ Begin, which will set SDWN, send a \$RSRF to the Control Frame, and enter a delay line to emerge as \$IFR. During the time interval between SDWN set and \$IFR the following events occur:

- 1) SDC comes true.
- 2) ϕ DSBR₁₉₋₂₆/BC₄₋₁₁ and ϕ ZBRX₀₋₁₁/BC₀₋₁₁ come true allowing the boundary check to be made.
- 3) ϕ DSBR₀₋₁₇/RS₀₋₁₇, ϕ ZBRX₀₋₁₁/RS₆₋₁₇, ϕ RS₀₋₁₇/ADR₀₋₁₇, and ϕ ZBRX₁₂₋₁₇/ADR₁₈₋₂₃ all come true causing the page and word number in the procedure Base Register to be added to the DSBR producing the address, in core memory, of the SDW.

\$IFR will set the IFR flip-flop in the Interface Frame. At this time SDC, PIN, and IFR will cause a last pulse detector to generate a \$A, which will:

- 1) Generate a \$ALS, which will reset IFR in the Interface Frame.
- 2) Generate a \$INT if there isn't an Out of Bounds Fault, or an Access Violation.
- 3) Generate a \$ADR, which will strobe the address into ADR₀₋₂₃

\$INT is sent to the selected Memory Controller and it will:

- 1) Reset PIN.
- 2) Set WAW.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-29 Sh. No.10-28

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.3.2 - contd

The Interface Frame will now wait until the Memory Controller acknowledges the request by sending a \$PIN. This pulse will be sent on to the Control Frame and delayed before it sets PIN, and is sent on to the Base Frame. When the Memory Controller has placed the SDW on the ZDI lines it will send a \$DA. This pulse will be forwarded on to the Base and Control Frames and it will enter a delay line to emerge and generate \$I, \$IS, and \$DES.

\$I samples the reset side of all the appending control flip-flops. In this case it will reset WAW, SDWN, and LPF.

\$IS samples the set side of all the appending control flip-flops. In this case it will set FANP, and it will issue a \$FAN, which is sent to the Control Frame as \$SSRF. It will also enter a delay line to emerge as \$IFR, which will set IFR.

\$DES will strobe the SDW on the ZDI lines into the Descriptor Register.

The ZDI₂₉₋₃₅ lines are routed through the Descriptor Generator. However, in this case no changes will be made to the descriptor field of the SDW before it is strobed into DES₂₉₋₃₅. The descriptor field on the ZDI lines will be checked for a directed fault, and as soon as FANP is set, the descriptor field in the Descriptor Register will be checked for class faults.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-30 Sh. No. 10-29

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.3.2 - contd

During the time interval between FANP set and \$IFR the following events occur:

- 1) \$IFF will be sent to the Control Frame to set its IFR flip-flop.
- 2) SDC goes false.
- 3) FA will come true.
- 4) $\phi BS_{0-11}/BC_{0-11}$ and DES_{19-26}/BC_{4-11} come true allowing the boundary check to be made.
- 5) $\phi DES_{0-17}/RS_{0-17}$, $\phi BS_{0-11}/RS_{6-17}$, $\phi RS_{0-17}/ADR_{0-17}$, and $\phi BS_{12-17}/ADR_{18-23}$ all come true causing the word number of the effective address to be added to the SDW producing the address, in core memory, of the instruction pair.
- 6) \$IFR will set the IFR flip-flop in the Interface Frame.

When the three related frames are ready, as signified by BFR, CFR, and IFR being set, FA is true, and PIN is set, a last pulse detector will generate a \$A, which will:

- 1) Generate a \$ALS, which will reset IFR and FANP.
- 2) Generate a \$INT if there isn't an Out of Bounds fault or AVF.
- 3) Reset BFR and CFR.
- 4) Generate a \$ADR which will strobe the address into ADR_{0-23} .

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-31 Sh. No.10-30

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.3.2 - contd

\$INT is sent to the selected Memory Controller and it will:

- 1) Reset PIN.

The Interface Frame will now wait until the Memory Controller acknowledges the request. Since this is a request for an instruction pair the Memory Controller will send two \$PINs and two \$DAs. The instruction pair will be placed on the ZDI lines. The \$PINs and the \$DAs will be forwarded on to the Base and Control Frames. This completes this particular operation.

Assume that it is not a Base instruction, the Segment Descriptor Table is paged and that an operand is to be stored in a large page. (DSBR₂₇"1", DSBR₂₈"0", SDW₂₇"0" and SDW₂₈"0" the base bit is on). After the Control Frame has embarked on a prepare address cycle, it will send a \$SAP to the Interface Frame.

\$SAP will generate a \$ Begin, which will set DSPTW, send a \$RSRF to the CF, and enter a delay line to emerge as \$IFR. During the time interval between DSPTW set and \$IFR the following events occur:

- 1) SDC comes true.
- 2) ϕ ZBRX₀₋₁₁/BC₀₋₁₁ and ϕ DSBR₁₉₋₂₆/BC₄₋₁₁ come true allowing the boundary check to be made.
- 3) ϕ DSBR₀₋₁₇/RS₀₋₁₇, ϕ ZBRX₄₋₁₁/RS₁₆₋₁₇, ADR₁₈₋₂₃, and ϕ RS₀₋₁₇/ADR₀₋₁₇ come true causing the page number in the Procedure Base Register to be added to the DSBR producing the address, in core memory, of the DSPTW.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-32 Sh. No. 10-31

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.3.2 - contd

\$IFR will set the IFR flip-flop in the Interface Frame. At this time SDC, PIN, and IFR will cause a last pulse detector to generate a \$A, which will:

- 1) Generate a \$ALS, which will reset IFR in the Interface Frame.
- 2) Generate a \$INT if there isn't an Out of Bounds Fault, or AVF.
- 3) Generate a \$ADR that will strobe the address into ADR₀₋₂₃.

\$INT is sent to the selected Memory Controller and it will:

- 1) Reset PIN.
- 2) Set WAW.

The Interface Frame will now wait until the Memory Controller acknowledges the request by sending a \$PIN. This pulse will be sent on to the Control Frame and delayed before it sets PIN and is sent on to the Base Frame. When the Memory Controller has placed the DSPTW on the ZDI lines it will send a \$DA. This pulse will be sent on to the Base and Control Frames and it will enter a delay line to emerge and generate \$I, \$IS, and \$DES.

\$I samples the reset side of all the appending control flip-flops. In this case it will reset DSPTW and WAW.

\$IS samples the set side of the appending control flip-flops. In this case it will set SDWP and enter a delay line to emerge as \$IFR, which will set IFR.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-33 Sh. No.10-32

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.3.2 - contd

\$DES will strobe the DSPTW on the ZDI lines into the Descriptor Register.

The ZDI₂₉₋₃₅ lines are routed through the Descriptor Generator. However, in this case, no changes will be made to the descriptor field of the DSPTW before it is strobed into DES₂₉₋₃₅. The descriptor field on the ZDI lines will be checked for a directed fault.

During the time interval between SDWP set and \$IFR the following event occurs:

- 1) $\phi ZBRX_{12-17}/ADR_{18-23}$, $\phi DES_{0-17}/RS_{0-17}$, and $\phi RS_{0-17}/ADR_{0-17}$ will come true concatenating the word number in the Procedure Base Register to the DSPTW in the Descriptor Register producing the address, in core memory, of the SDW.

\$IFR will set IFR in the Interface Frame. At this time SDC, PIN, and IFR will cause a last pulse detector to generate a \$A, which will:

- 1) Generate a \$ALS, which will reset IFR.
- 2) Generate a \$INT.
- 3) Generate a \$ADR that will strobe the address into ADR₀₋₂₃.

The Interface Frame will now wait until the Memory Controller acknowledges the request by sending a \$PIN. This pulse will be sent on to the Control Frame and delayed before it sets PIN and is sent on to the Base Frame. When the Memory Controller has placed the SDW on the ZDI lines it will send a \$DA. This pulse will be sent on to the Base and Control Frames and it will enter a delay line to emerge and generate \$I, \$IS, and \$DES.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-34 Sh. No. 10-33

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.3.2- contd

\$I samples the reset side of the appending control flip-flops. In this case, it will reset SDWP and WAW.

\$IS samples the set side of the appending control flip-flops. In this case it will set PTW and LPF and enter a delay line to emerge as \$IFR.

\$DES will strobe the SDW on the ZDI lines into the Descriptor Register. The descriptor field will not be altered, but it will be checked for a directed fault or an illegal class fault.

During the time interval between PTW set and \$IFR the following events occur:

- 1) $\phi BS_{0-7}/BC_{4-11}$ and $\phi DES_{19-26}/BC_{4-11}$ will come true allowing the boundary check to be made.
- 2) $\phi DES_{0-17}/RS_{0-17}$, $\phi RS_{0-17}/ADR_{0-17}$, and $\phi BS_{0-7}/RS_{16-17}$, ADR_{18-23} will come true concatenating the page number from the effective address to the SDW producing the address, in core memory of the PTW.

\$IFR will set IFR. At this time SDC, PIN and IFR will cause a last pulse detector to generate a \$A, which will:

- 1) Generate a \$ALS which will reset IFR.
- 2) Generate a \$INT if there isn't an Out of Bounds Fault, or AVF.
- 3) Generate a \$ADR, which will strobe the address into ADR_{0-23} .

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-35 Sh. No. 10-34

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.3.2 - contd

\$INT is sent to the selected Memory Controller and it will:

- 1) Reset PIN.
- 2) Set WAW.

The Interface Frame will now wait until the Memory Controller acknowledges the request by sending a \$PIN. This pulse will be sent on to the Control Frame and delayed before it sets PIN and is sent on to the Base Frame. When the Memory Controller has placed the PTW on the ZDI lines, it will send a \$DA. This pulse will be sent on to the Base and Control Frames, and it will enter a delay line to emerge and generate \$I, \$IS, and \$DES.

\$I samples the reset side of the appending control flip-flops. In this case it will reset PTW and WAW.

\$IS samples the set side of the appending control flip-flops. In this case it will set FAPM and enter a delay line to emerge as \$IFR.

\$DES will strobe the PTW on the ZDI lines into the Descriptor Register. In this case a descriptor field will be generated for the PTW by the Descriptor Generator before it is strobed into DES²⁷⁻³⁵. (See paragraph 10.1.4.2 on the Descriptor Generator for a description of this operation.) The descriptor field will be checked for directed faults, illegal class faults, or access violations.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-36 Sh. No.10-35

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.3.2 - contd

During the time interval between FAPM set and \$IFR the following events occur:

- 1) \$IFF will be sent to the Control Frame to set its IFR flip-flop.
- 2) SDC goes false.
- 3) FA and EA will come true.
- 4) $\phi DES_{0-17}/RS_{0-17}$, $\phi PS_{0-13}/ADR_{0-13}$ and BS_{8-11}/ADR_{14-17} , and $\phi BS_{12-17}/ADR_{18-23}$ will come true concatenating the word number of the effective address to the PTW producing the address, in core memory, of the location in which the operand is to be stored.
- 5) \$IFR will set IFR.

When the three related frames are ready, as signified by BFR, CFR, and IFR set, FA true, and PIN set a last pulse detector will generate a \$A, which will:

- 1) Generate \$ALS, which will reset FAPM and IFR.
- 2) Generate a \$INT.
- 3) Reset BFR and CFR.
- 4) Generate a \$ADR, which will strobe the address into ADR_{0-23} .

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-37 Sh. No. 10-36

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.3.2 - contd

\$INT is sent to the selected Memory Controller and it will:

- 1) Reset PIN.
- 2) Generate a \$DS, which is sent to the AF, CF, and BF.

The operand will be stored in the address specified by the Address Register, thus completing this operation.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-38 Sh. No. 10-37

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.3.3 Append with Associative Memory

This mode of operation is characterized by the Interface Frame being controlled by the Associative Memory. It will set up for a particular type of operation, and then it will proceed with it or change to a new type upon command of the Associative Memory. This will be the mode of operation normally used.

The Associative Memory can store up to 16 SDWs or PTWs. At the start of an appending cycle it is searched for the required SDW or PTW. If either one is found, it will be used eliminating the need for a core memory access. If the required SDW or PTW is not found it will be obtained from core memory and stored in the Associative Memory, where it can be accessed the next time it is needed. There are five possible outcomes of an Associative Memory search, plus an additional special case involving the written bit. They are:

- 1) No information available.
- 2) No information available after a pointer match.
- 3) Nonpaged SDW found.
- 4) Paged SDW found.
- 5) PTW found.

See section 11.0 on the Associative Memory for the details of the search operation and the development of the various pulses. In the following discussions it will be assumed that all appending control flip-flops are reset at the start of the cycle, that a \$AAM has been received from the Control Frame setting AMS and FANP, and that the Associative Memory has started its search.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-39 Sh. No. 10-38

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.3.3 - contd

- 1) If the search is unsuccessful the Associative Memory will send a \$NIA which will:

- a) Reset AMS.
- b) Generate a \$ RESTART.
- c) Generate a \$ BEGIN.

\$ RESTART will reset FANP.

\$ BEGIN will start an appending cycle that is the same as started by a \$SAP from the Control Frame, except that SDWs or PTWs retrieved from core memory will be stored in the Associative Memory.

- 2) If the search produces a pointer match (paged and no SDW present) the Associative Memory will send either a \$PFLP (QSUL1) or a \$PFSP (QSUS1). Either pulse will reset FANP and set FAPM. \$PFLP will set LPF. \$PFSP will reset LPF. If the search produces no further match the Associative Memory will send a \$NIA, which will:

- a) Reset AMS.
- b) Generate a \$ RESTART, which will reset FAPM.
- c) Generate a \$ BEGIN.

\$ BEGIN will start an appending cycle that is the same as started by a \$SAP from the Control Frame.

- 3) If the search produces a match with a nonpaged SDW (bit 28 = 1) (64 words) the Associative Memory will send a \$GO (QSSF1). The Interface Frame is set up in the Final Address Nonpaged mode. \$GO will reset LPF and enter a delay line to emerge and generate \$IFR.

COMPANY CONFIDENTIAL

GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-40 Sh. No.10-39

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.3.3 - contd

During the time interval between \$GO and \$IFR the following events occur:

- a) FA, EA, and FAN will come true.
- b) \$IFF is sent to the Control Frame to set its IFR flip-flop.
- c) ϕ BS₀₋₁₁/BC₀₋₁₁ and ϕ ZABD₁₉₋₂₆ and BC₄₋₁₁ will come true allowing the boundary check to be made.
- d) ϕ ZASM₁₂₋₁₇/ADR₁₈₋₂₃ will come true causing the combined page and word number of the effective address to be added to the SDW, from the Associative Memory, producing the address of the operand.

\$IFR will set IFR.

From this point on the Interface Frame will proceed the same as it did when it did not use the Associative Memory. The first \$A will reset AMS.

- 4) If the search produces a match with a paged SDW (1024 words) the sequence of events will be as follows.

At the end of the pointer search the Associative Memory will send a \$PFLP (QSUL1), which will:

- a) Reset FANP.
- b) Set FAPM and LPF.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-41 Sh. No.10-40

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.3.3 - contd

At the end of the PTW search, where no match is found, the Associative Memory will send a \$GO (QSSF1), which will enter a delay line to emerge and generate \$IFR.

During the time interval between \$GO and \$IFR the following events occur:

- a) $\phi BS_{0-7}/BC_{4-11}$ and $\phi ZABD_{19-26}/BC_{4-11}$ will come true allowing the boundary check to be made.
- b) $\phi ZASM_{0-17}/RS_{0-17}$, $\phi BS_{0-17}/RS_{16-17}$, ADR_{18-23} , and $\phi RS_{0-17}/ADR_{0-17}$ will come true adding the page number from BS to the SDW producing the address of the PTW.

\$IFR will set IFR.

From this point on the Interface Frame will proceed the same as it did when it did not use the Associative Memory. The first \$I will reset AMS.

- 5) If the search produces a match with a small PTW (64 words) the sequence of events will be as follows.

At the end of the pointer search the Associative Memory will send a \$PFSP (QSUS1), which will:

- a) Reset FANP.
- b) Set FAPM.

At the end of the PTW search the Associative Memory will send a \$GO (QSSF1) which will enter a delay line to emerge and generate a \$IFR.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-42 Sh. No.10-41

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.3.3 - contd

During the time interval between \$GO and \$IFR the following events occur.

- a) FA, EA, and FAN will come true.
- b) \$IFF will be sent to the Control Frame to set its IFR flip-flop.
- c) $\phi ZASM_0-13/ADR_0-13$, $\phi ZASM_{14-17}/ADR_{11-17}$, and $\phi BS_{12-17}/ADR_{18-23}$ will come true concatenating the word number from the effective address to the PTW from the Associative Memory, producing the address of the operand.

\$IFR will set IFR.

From this point on the Interface Frame will proceed the same as it did when it did not use the Associative Memory. The first \$A will reset AMS.

This concludes the address preparation except for special conditions which will be considered next.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-43 Sh. No. 10-42

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.4 SPECIAL OPERATION

Items to be discussed under this general heading are Written and Use bits, Descriptor Generator, Base Instructions, and Multiple Load Store Operation.

10.1.4.1 Written and Use Bits

It is necessary to be able to tell if a page in core memory has been used or if it has been altered by looking at its PTW. Two bits (25 and 26) are reserved for this purpose. If bit 25 (Use bit) is a "1" the page has been used. If bit 26 (Written bit) is a "1" the page has been altered. When a page is initially stored in core memory and its PTW created both bits will be a "0." The first time the page is accessed or written into the corresponding bit of the PTW in both core memory and the Associative Memory will be made a "1."

Assume that the Interface Frame has just issued a \$INT for a PTW, it is a store operation, and bits 25 and 26 are both "0." The Memory Controller will place the PTW on the ZDI lines and then send a \$DA. This pulse will be sent to the Base and Control Frames and it will enter a delayline to emerge and generate \$I, \$IS, and \$DES.

\$I samples the reset side of the appending control flip-flops. In this case it will reset PTW and WAW.

\$IS samples the set side of the appending control flip-flops. In this case it will set SWU, WBF, and enter a delayline to emerge as \$IFR.

\$DES will strobe the PTW on the ZDI lines into the Descriptor Register. In this case a descriptor field will be generated for the PTW and bit 29 will be forced to a "1" by the Descriptor Generator before it is strobed into DES₂₇₋₃₅. The Descriptor field will be checked for directed faults, illegal class faults, and access violations.

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PHOENIX, ARIZONA

Spec. No. M50EB00107
Cont. on Sh.10-44 Sh. No.10-43

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.4.1 - contd

During the time interval between SWU and \$IFR the following events occur:

- 1) SDC goes false.
- 2) A clear-write command to core memory is prepared.
- 3) The Zone Register is set to 00000100, which will cause only bits 24, 25, and 26 to be altered.
- 4) A "1" is placed on data out lines 25 and 26.

\$IFR will set IFR. At this time SWU, PIN, and IFR will cause a last pulse detector to generate a \$A, which will:

- 1) Generate a \$ALS, which will reset IFR.
- 2) Generate a \$INT.
- 3) Generate a \$ADR, which is inhibited from strobing ADR₀₋₂₃ by SWU.

\$INT is sent to the selected Memory Controller and it will:

- 1) Cause a "1" to be written into bits 25 and 26 of the PTW in core memory.
- 2) Reset PIN.
- 3) Set WAW.

The Interface Frame will now wait until the Memory Controller acknowledges the request by sending a \$PIN. This pulse will be sent on to the Control Frame and delayed before it sets PIN and is sent on the Base Frame.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-45 Sh. No. 10-44

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.4.1- contd

When the Memory Controller has completed the clear-write operation it will send a \$DA. This pulse will be sent to the Base and Control Frames, and it will enter a delay line to emerge and generate \$I and \$IS.

\$I samples the reset side of the appending control flip-flops. In this case it will reset SWU, WBF, and WAW.

\$ITS samples the set side of the appending control flip-flops. In this case it will set FAPM and enter a delay line to emerge as \$IFR. From this point on it will continue the same as for any FAPM cycle.

The same cycle will be gone through if only bit 25 or bit 26 need to be made a "1."

One other possibility exists, and that is that a PTW with the Written bit a "0" is found in the Associative Memory during a store or RAR operation.

When a store or RAR operation is decoded, the Interface Frame places a "1" on the BMST1 line to the Associative Memory. If a PTW with the Written bit a "0" is found the Associative Memory will send the Interface Frame a \$SWBC (QWBC1) instead of the \$GO (QSSF1). \$SWBC will set WBS and generate a \$ RESTART.

WBS set will place a "1" on the BWSB1 line to the Associative Memory, which will cause it to make its Written bit a "1."

\$ RESTART will reset FAPM and generate a \$ BEGIN.

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GENERAL ELECTRIC COMPANY
COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-46 Sh. No.10-45

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.4.1 - contd

\$ BEGIN will strobe DWPTW and SDWN. If the Descriptor Table is paged DSPTW will set, otherwise SDWN will set. Assume that SDWN set. \$ BEGIN will also send a \$RSRF to the Control Frame and enter a delay line to emerge as \$IFR. During the time interval between SDWN set and \$IFR the following events occur:

- 1) SDC come true.
- 2) ϕ DSBR₁₉₋₂₆/BC₄₋₁₁ and ZBRX₀₋₁₁/BC₀₋₁₁ come true allowing the boundary check to be made.
- 3) ϕ DSBR₀₋₁₇/RS₀₋₁₇, ϕ ZBRX₀₋₁₁/RS₆₋₁₇, ϕ RS₀₋₁₇/ADR₀₋₁₇, and ϕ ZBRX₁₂₋₁₇/ADR₁₈₋₂₃ all come true causing the page and word number in the Procedure Base Register to be added to the DSBP producing the address of the SDW.

\$IFR will set IFR. At this time SDC, PIN, and IFR will cause a last pulse detector to generate a \$A, which will:

- 1) Generate a \$ALS, which will reset IFR.
- 2) Generate a \$INT if there isn't an Out of Bounds fault.
- 3) Generate a \$ADR that will strobe the address into ADR₀₋₂₃.

\$INT is sent to the selected Memory Controller and it will:

- 1) Reset PIN.
- 2) Set WAW.

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COMPUTER EQUIPMENT DEPARTMENT
PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-47 Sh. No. 10-46

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.4.1 - contd

The Interface Frame will now wait until the Memory Controller acknowledges the request by sending a \$PIN. This pulse will be sent on to the Control Frame and delayed before it sets PIN and is sent on to the Base Frame. When the Memory Controller has placed the SDW on the ZDI lines it will send a \$DA. This pulse will be sent on to the Base and Control Frames and it will enter a delay line to emerge and generate \$I, \$IS, and \$DES.

\$I samples the reset side of the appending control flip-flops. In this case it will reset SDWN and WAW.

\$IS samples the set side of the appending control flip-flops. In this case it will set SWU and enter a delay line to emerge as \$IFR.

\$DES will strobe the SDW on the ZDI lines into the Descriptor Register. The descriptor field will not be altered but it will be checked for a Directed Fault or an Illegal Class Fault.

During the time interval between SWU and \$IFR the following events occur:

- 1) SDC goes false.
- 2) A clear-write command to core memory is issued.
- 3) The Zone Register is set to 00000100, which will cause only bits 24, 25, and 26 to be altered.
- 4) A "1" is placed on data out lines 25 and 26.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-48 Sh. No.10-47

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

10.1.4.1 - contd

\$IFR will set IFR. At this time SWU, PIN, and IFR will cause a last pulse detector to generate a \$A, which will:

- 1) Generate a \$ALS, which will reset IFR.
- 2) Generate a \$INT.
- 3) Generate a \$ADR, which will strobe the address into the Address Register.

\$INT is sent to the selected Memory Controller and it will:

- 1) Cause a "1" to be written into bits 25 and 26 of the PTW in core memory.
- 2) Reset PIN.
- 3) Set WAW.

The Interface Frame will now wait until the Memory Controller acknowledges the request by sending a \$PIN. This pulse will be sent on to the Control Frame and delayed before it sets PIN and is sent on to the Base Frame. When the Memory Controller has completed the clear-write operation it will send a \$DA. This pulse will be sent to the Base and Control Frames, and it will enter a delay line to emerge and generate \$I and \$IS.

\$I samples the reset side of the appending control flip-flops. In this case it will reset SWU, WBS, and WAW.

\$IS samples the set side of the appending control flip-flops. In this case it will set FAPM and enter a delay line to emerge as \$IFR.

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-49 Sh. No. 10-48

TITLE: ENGINEERING PRODUCT SPECIFICATION
 GE-645 PROTOTYPE PROCESSOR

10.1.4.1 - contd

During the time interval between FAPM set and \$IFR the following events occur:

- 1) \$IFF will be sent to the Control Frame to set its IFR flip-flop.
- 2) FA and possibly EA will come true.
- 3) $\phi ZASM_0-13/ADR_0-13$, $\phi ZASM_{14-17}/ADR_{14-17}$, and BS_{12-17}/ADR_{18-23} will all come true concatenating the word number of the effective address to the PTW from the Associative Memory to form the operand address.

\$IFR will set IFR.

From this point on it will continue as any final address cycle.

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GE-645 PROTOTYPE PROCESSOR

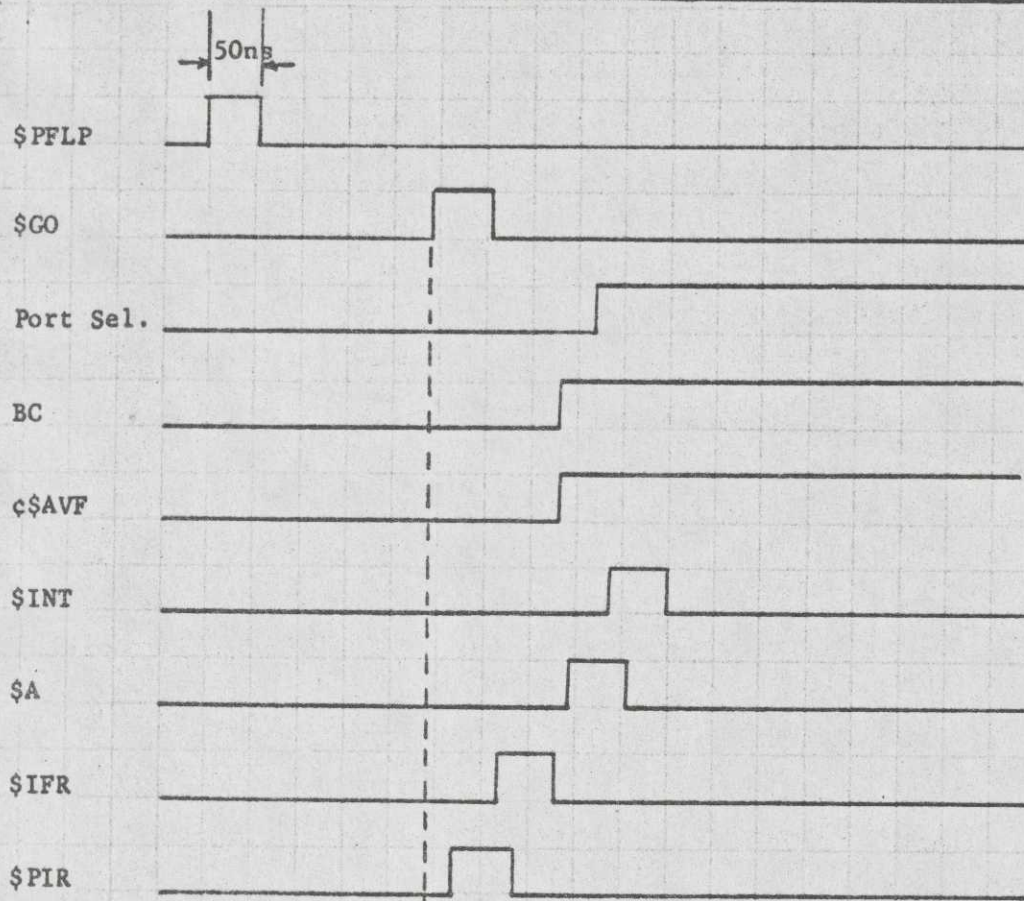


Fig. 10.1.4 FAPM (AMS) Mode, Timing Diagram

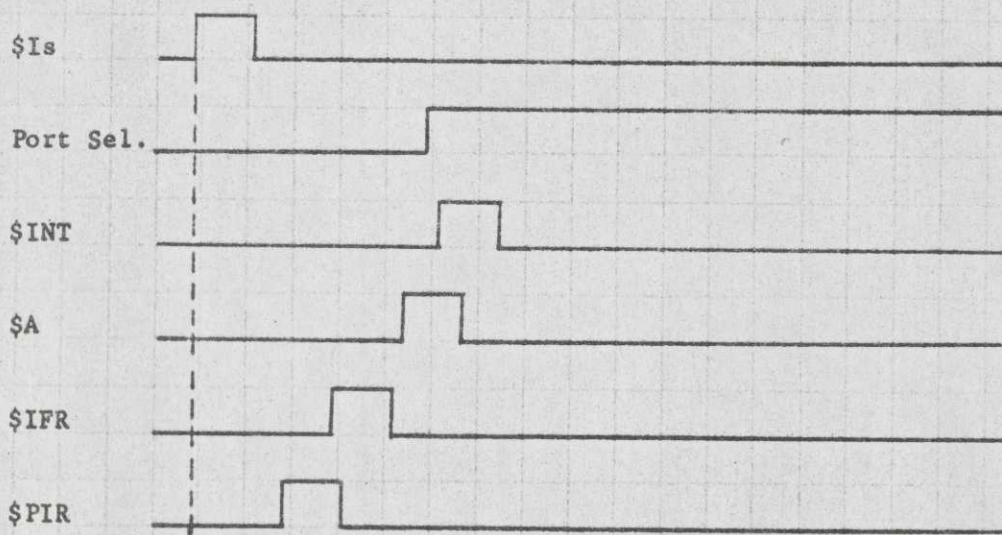


Fig. 10.1.4a SWU (WBS) Mode, Timing Diagram

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GE-645 PROTOTYPE PROCESSOR

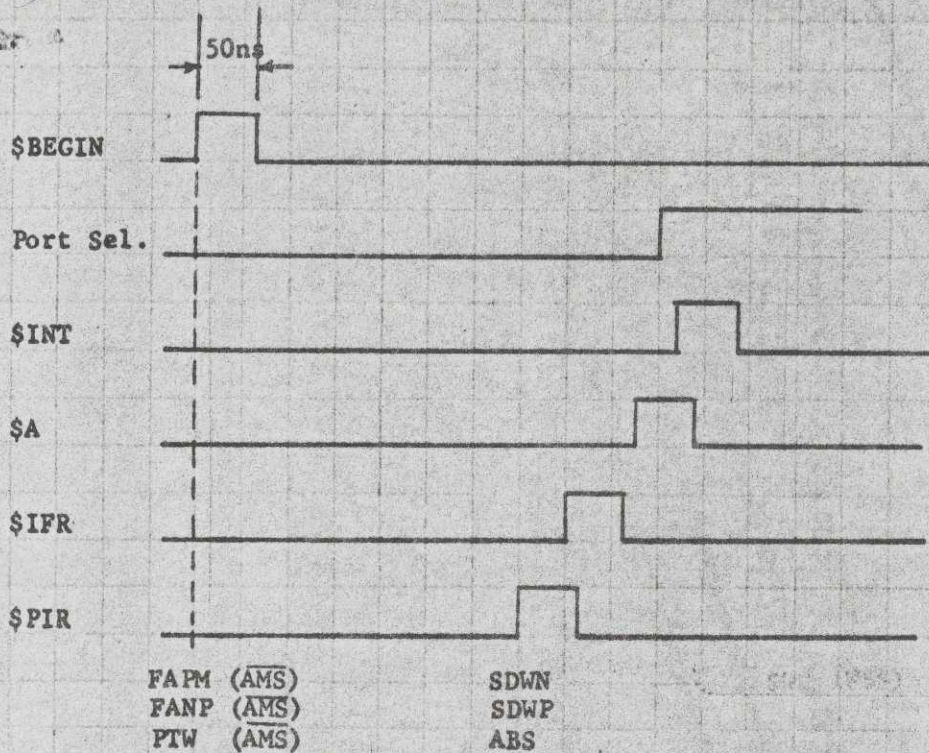


Fig. 10.1.4b SWU (WBS) Modes, Timing Diagram

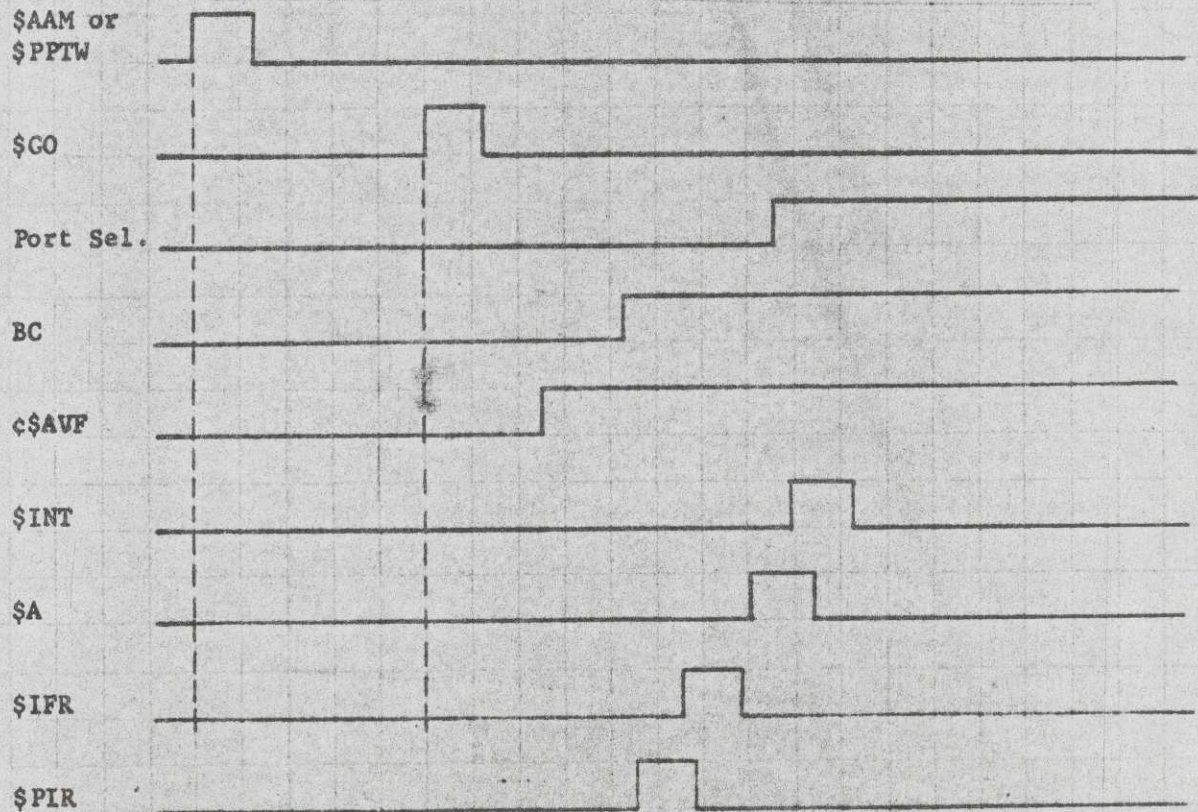


Fig. 10.1.4c FAN (AMS) or PTW (AMS) Modes, Timing Diagram

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 GE-645 PROTOTYPE PROCESSOR

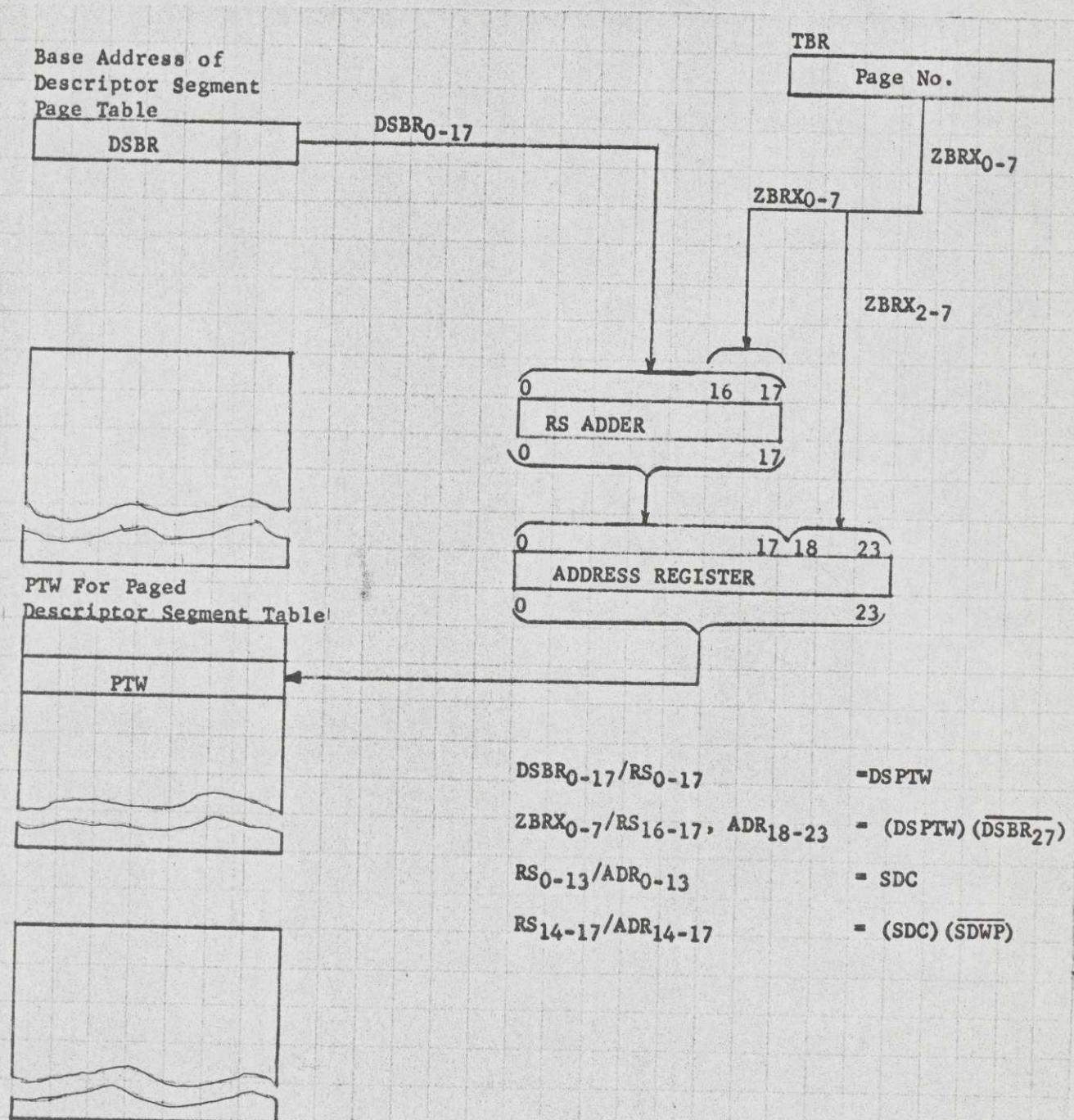


Fig. 10.1.4d Descriptor Segment Page Table Word Fetch - Large Page, Flow Chart

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh. 10-53 Sh. No.10-52

TITLE: ENGINEERING PRODUCT SPECIFICATION
GE-645 PROTOTYPE PROCESSOR

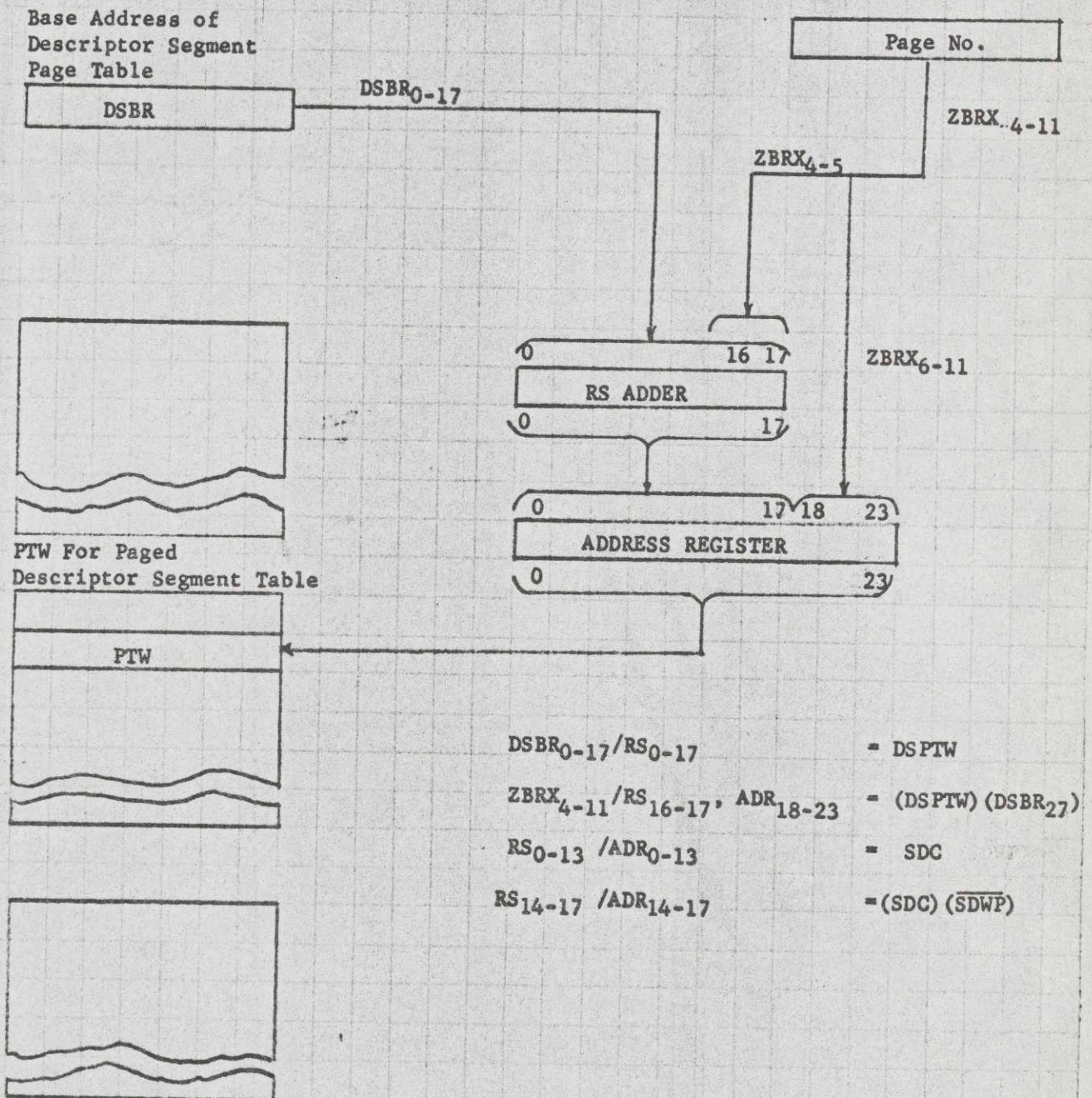


Fig. 10.1.4e Descriptor Segment Page Table Word Fetch - Small Page, Flow Chart

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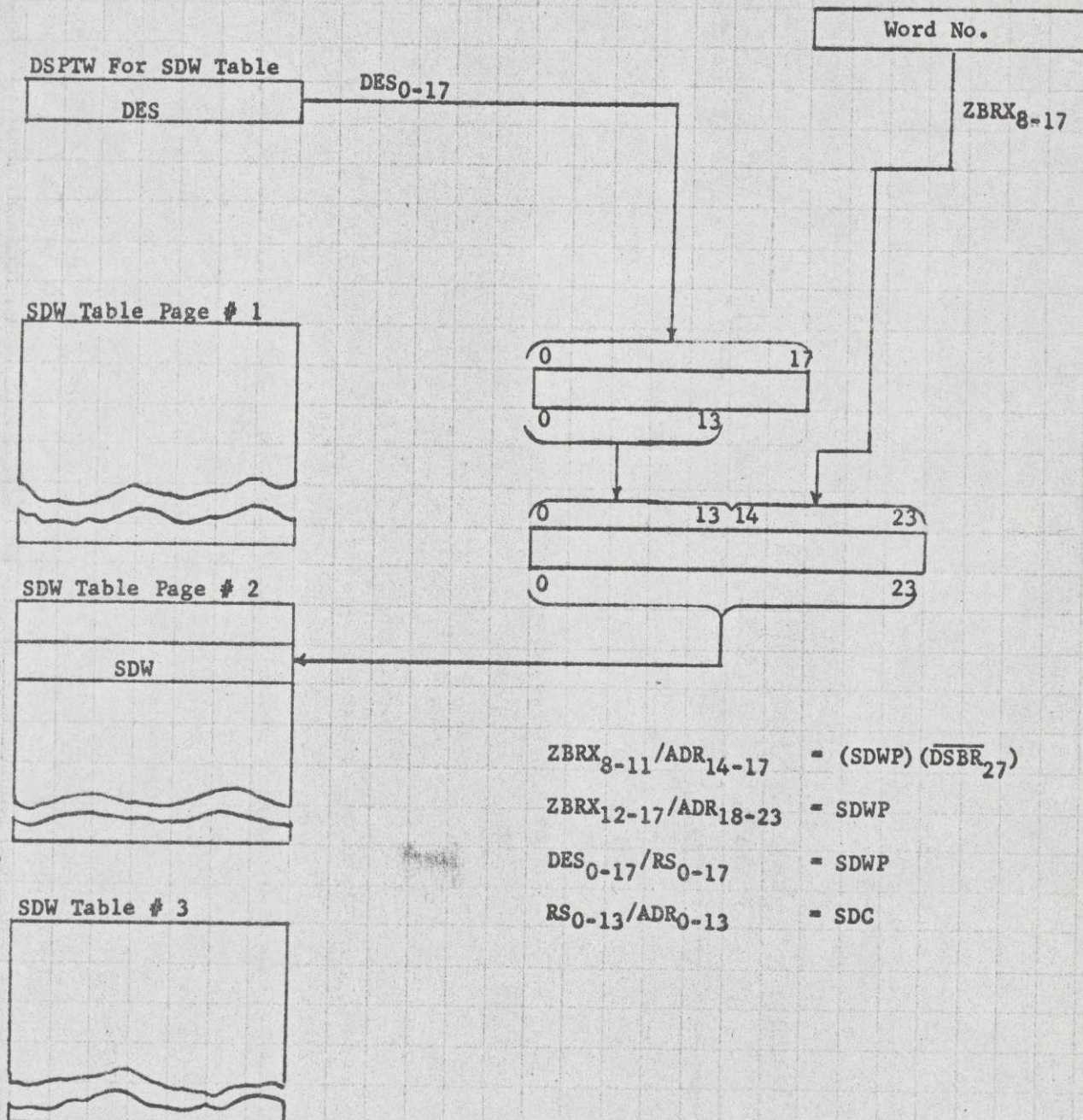


Fig. 10.1.4f SDW Fetch, Paged SWD Table (Large), Flow Chart

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PHOENIX, ARIZONA

Spec. No. M50EB00107

Cont. on Sh.10-55 Sh. No.10-54

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GE-645 PROTOTYPE PROCESSOR

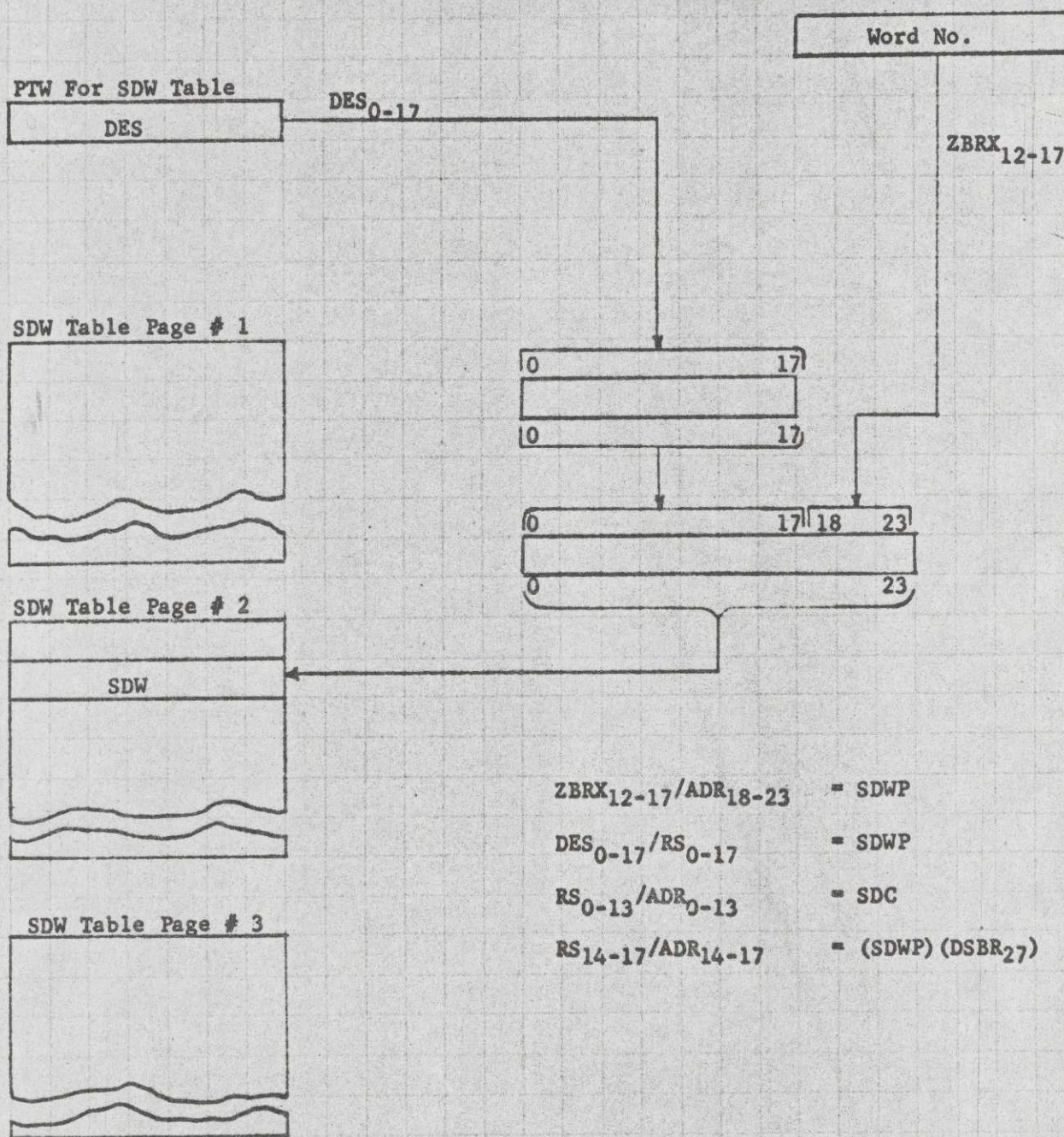


Fig. 10.1.4g SDW Fetch, Paged SWD Table (Small), Flow Chart

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Cont. on Sh.10-56 Sh. No.10-55

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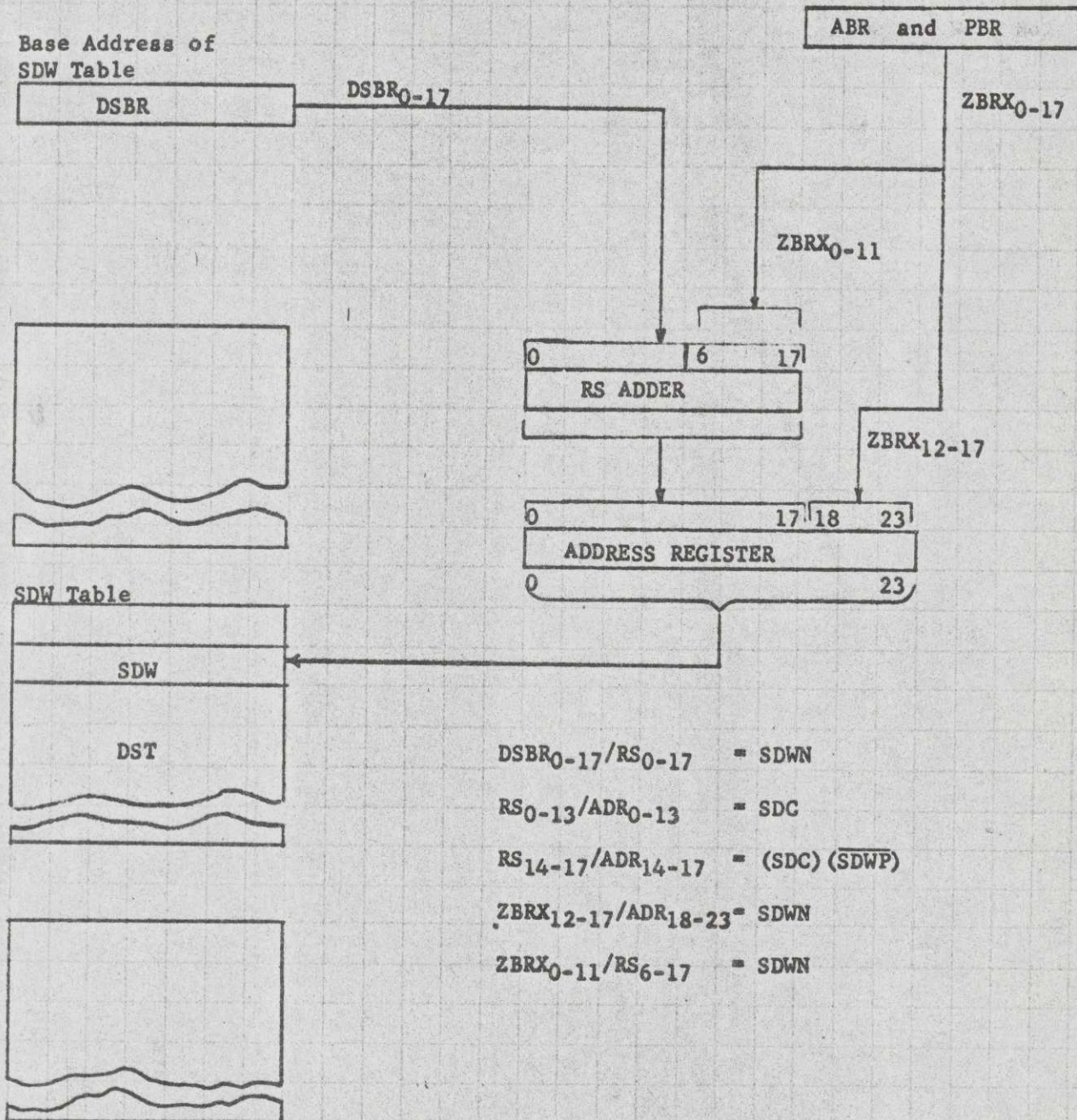


Fig. 10.1.4h SDW Fetch, Nonpaged, Descriptor Segment Flow Chart

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Spec. No. M50EB00107

Cont. on Sh.10-57 Sh. No.10-56

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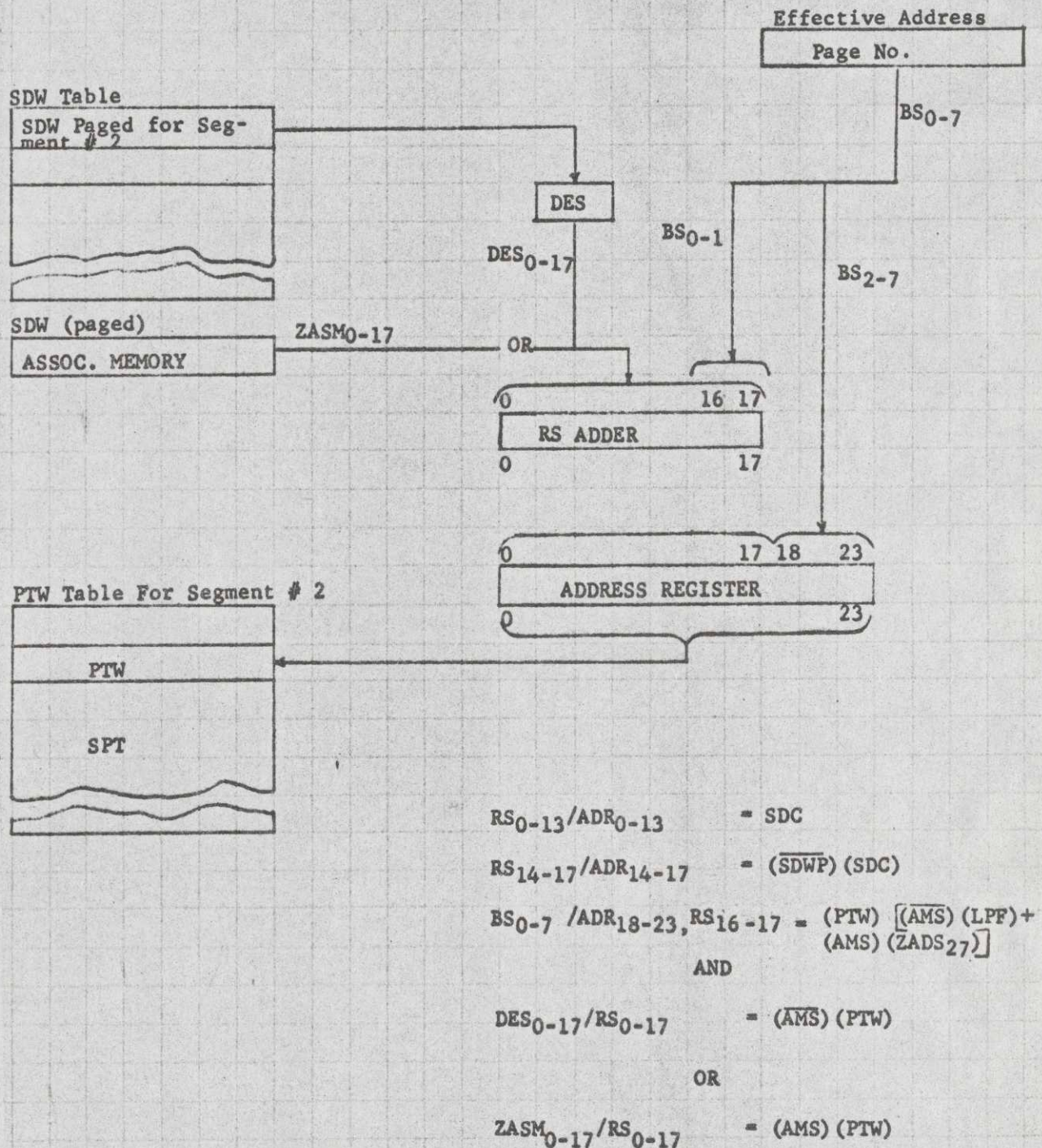


Fig. 10.1.41 Page Table Word Fetch - Large Page, Flow Chart

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 GE-645 PROTOTYPE PROCESSOR

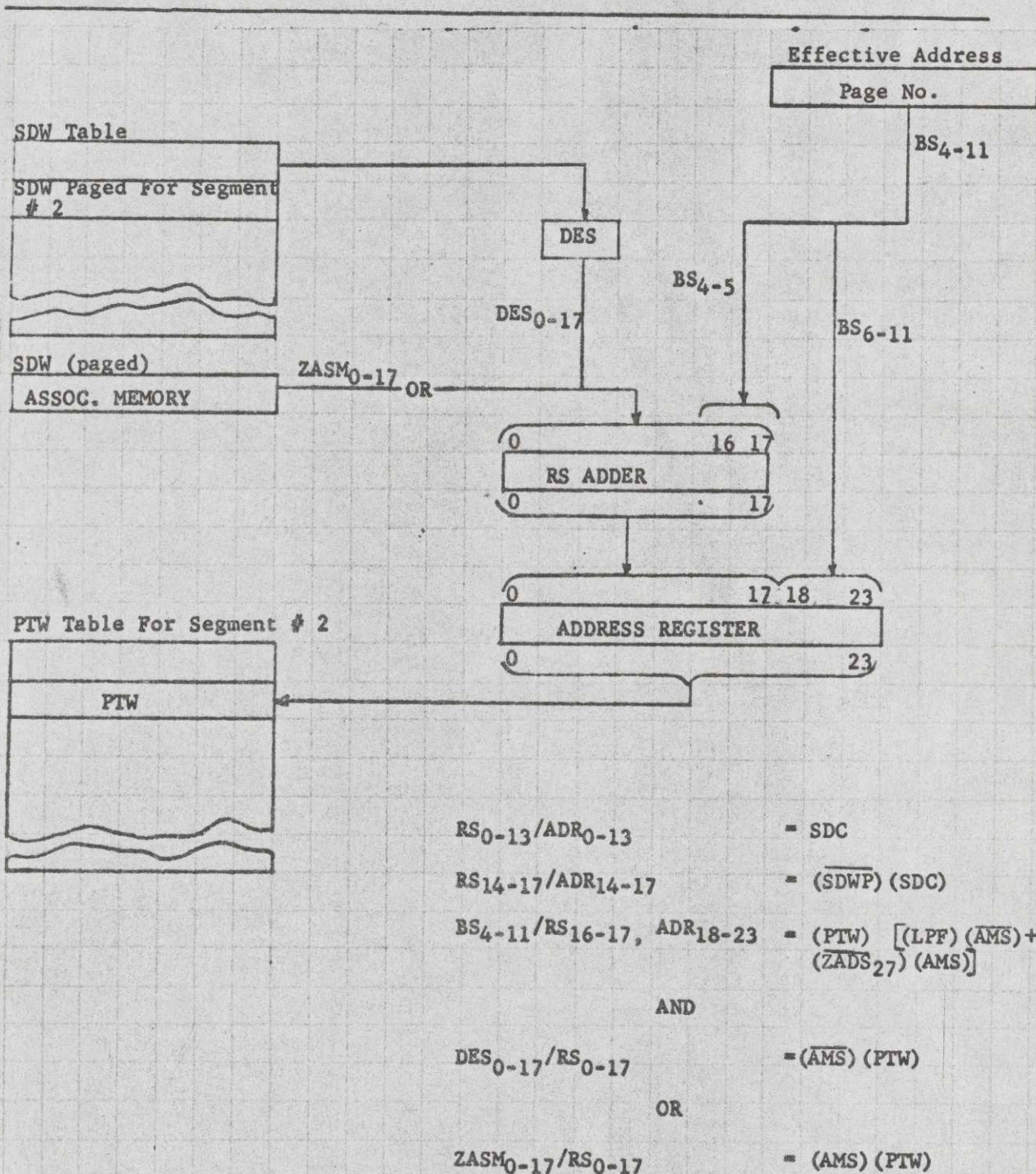


Fig. 10.1.4j Page Table Word Fetch - Small Page, Flow Chart